ADM-PA120
User Manual

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1 Introduction

The ADM-PA120 is a high-performance reconfigurable computing card featuring the latest AMD Adaptive Compute Acceleration Platform (ACAP) platform known as Versal. The PCIe form factor is ideal for Data Center applications and general evaluation and deployment of this architecture. The card features three QSFP-DD interfaces, four banks of 64-bit LPDDR4-SDRAM, front panel Ethernet, 1pps input, 10MHz input, trigger I/O, RJ45 ToD/1PPS, PMOD, and USB.

Figure 1 : ADM-PA120 Fully Assembled

1.1 Order Code

See the datasheet on web page https://www.alpha-data.com/product/adm-pa120/ for complete ordering options.

1.2 Key Features

Key Features

- PCIe Gen4 x16, dual Gen5x8 capable
- 2-slot active or passive heat sink
- 3/4 length, full profile, x16 edge PCIe form factor
- Supports Versal XCVP1202 and XCVP1502 ACAP devices in the VSVA2785 package
- 3x QSFP-DD interfaces at front panel
  - 2x QSFP-DD cages connected to GTM capable of 56g PAM4 on each of the 16 channels.
  - 1x QSFP-DD cage connected to GTY capable of 28g NRZ on each of the 8 channels.
- Industry standard low speed I/O at the front panel
  - SMA for 1PPS input
  - SMA for 10MHz input
  - SMA with Trig input/output
  - RJ45 with 2x bidirectional RS485 interfaces for ToD and 1PPS
- Versatile MIO interface support:
  - GEM0 Ethernet access through RJ45 at front panel
  - uSD
  - Dual QSPI
  - ULPI USB PHY accessible at USBA receptacle
  - 2x UART broken out through micro-USB at PCIe front panel and rear
- Four separate banks of 64 bit LPDDR4 SDRAM at 3900 MT/s for 3 banks 3200MT/s for 1 bank
- Front panel and rear edge JTAG access via USB port
- ACAP configurable over USB/JTAG and SPI configuration flash
- Voltage, current, and temperature monitoring
- Digilent PMOD 3.3V, 12-pin interface accessible to PL
- 6 user LEDs

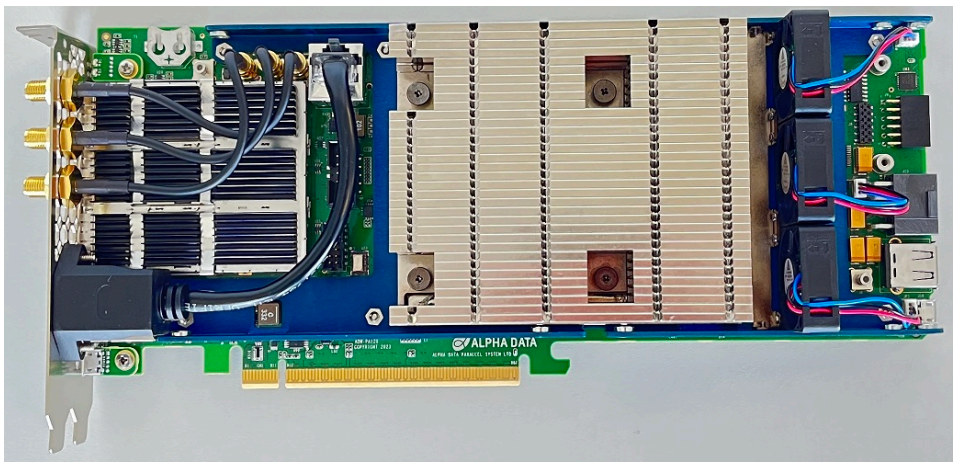


Figure 2 : ADM-PA120 Product Photo

2 Board Information

2.1 Physical Specifications

The ADM-PA120 complies with PCI Express CEM revision 5.0.

Description	Measure
PCB Dy	111.15 mm
PCB Dx	254 mm
Total Dz	19.9 mm

Table 1 : Mechanical Dimensions (PCB only)

Description	Measure
Total Dy	126.3 mm
Total Dx	267.5 mm
Total Dz	41.9 mm
Total weight	865 grams
Weight of PCIe handle	30 grams

Table 2 : Mechanical Dimensions (Fully Assembled)

The total weight does not include the PCIe Handle, which is optional, and shipped uninstalled.

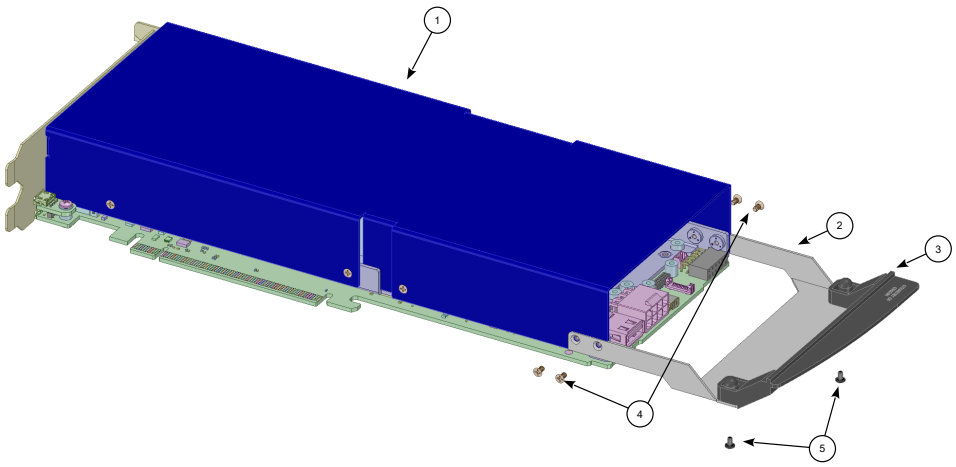
2.2 PCIe Handle Installation

The ADM-PA120 ships fully assembled. There is a PCIe-compliant handle shipped in a separate bag within the product package. This handle assembly includes a plastic handle and a metal bracket. The bracket simulates the full-length PCIe card length and frequently lines up with server retention clips. The plastic handle can be removed and only the metal bracket used if it fits better in the host system. Use all retention options available to secure this add-in card.

The drawing below details the installation of the rear handle bracket.

ITEM	PART NO	DESCRIPTION	QTY	MANUFACTURER/DISTRIBUTOR
1	ADM-PA120	ADM-PA120 (AD01492), PCIE, ASSEMBLY	1	ALPHA DATA
2	AD01398-1_SP05-3	HANDLE SUPPORT BRACKET (GOMPF P/N 3200-2954LC ECO 02)	1	GOMPF
3	91060000AFG	PCIE HANDLE	1	GOMPF
4	92010A001	SCREW, M2 X 4MM, FLAT HEAD, STAINLESS STEEL	4	MCMASTER-CARR / GENERIC
5	6089-3512	SCREW, SELF-THREADING, PAN HEAD, STAINLESS STEEL	2	GOMPF

REV	ZONE	DESCRIPTION	DATE	DWN BY
1	ALL	INITIAL RELEASE	26-MAY-2023	K. ROTH



NOTES

1. USE LOCTITE 222 ON ALL SCREWS
2. TORQUE ALL SCREWS TO 0.23N-M [2IN-LBS].
3. SUGGESTED ASSEMBLY ORDER FOLLOWS ITEM NUMBER IN ASCENDING ORDER.
4. START ALL SCREW SETS LOOSELY BEFORE TIGHTENING GROUP.

Alpha Data Parallel Systems Ltd
160 Dundee Street
Edinburgh, EH11 1DQ, UK
www.alpha-data.com

Title: ADM-PA120 Support Bracket Assembly
Size: A2 | Document No.: AD01492-1_FA02-1 | Rev:
Date: | Sheet: 1 of 1

Figure 3 : ADM-PA120 PCIe Handle Installation

2.3 Chassis Requirements

2.3.1 Handling Instructions

The components on this board can be damaged by electrostatic discharge (ESD). To prevent damage, observe ESD precautions:

- Always wear a wrist-strap when handling the card
- Hold the board by the edges
- Avoid touching any components
- Store in ESD safe bag.

2.3.2 PCI Express

The ADM-PA120 is capable of PCIe Gen 1/2/3/4 with 1/4/8/16-lanes, and PCIe Gen 5 with 1/4/8-lanes when using the AMD Integrated Block for PCI Express. PCIe Gen 5x8 can be bifurcated into two slots to achieve an aggregate bandwidth of a 16 lane connection.

2.3.3 Installation Instructions

Follow host server user guides and installation instructions. The steps below are a general guide, and should be superseded by host system instructions.

A 16-lane physical PCIe slot is required for mechanical compatibility.

The card is also designed to use the extra mechanical retention mechanisms defined in the PCIe specification. This includes both the board keep-out region along the top edge, and the full-length handle support. It is recommended to use all board retention features supported by the host systems. These cards are heavy and can be damaged when used in systems that do not mechanically support the hardware properly. The following instructions use each retention method. If a system lacks a particular retention mechanism, the user must skip that step and understand the risk of mechanical damage is higher than if the clips were included.

This equipment is not suitable for use in locations where children are likely to be present.

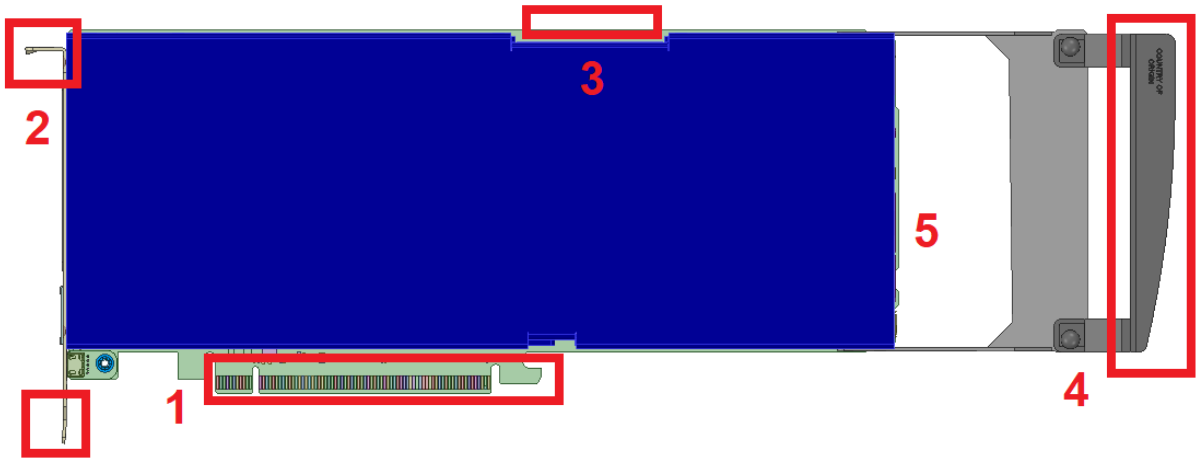


Figure 4 : Installation Steps

Installation Instructions

1 Ensure system power is off. Then hold the PCIe card securely above the PCIe slot in the system and push it straight into the connector. If the card is going onto a riser card, the riser card will need to be removed first.

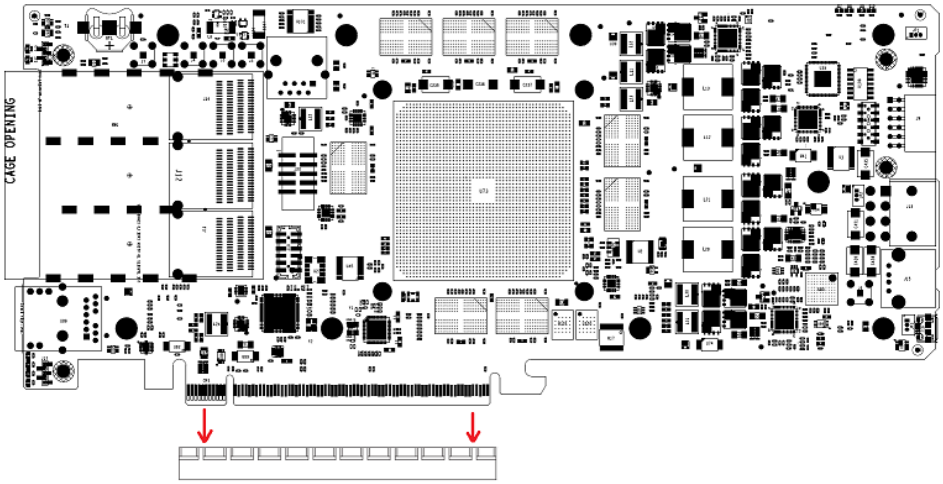


Figure 5 : Step 1) Plug In Card

2 Use the system screws or clip mechanism to secure the top of the front bracket at both hole positions.

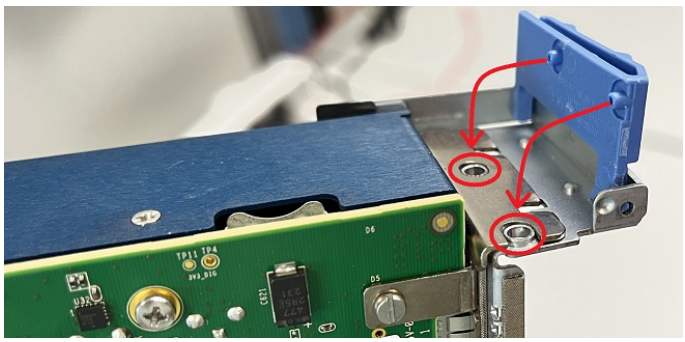


Figure 6 : Step 2) Secure Front Panel

3 Engage any system clips along the north edge to help secure the card.

4 Engage any system clips along the rear edge to help secure the card. You might need to remove the plastic handle to enable the clip to engage fully.

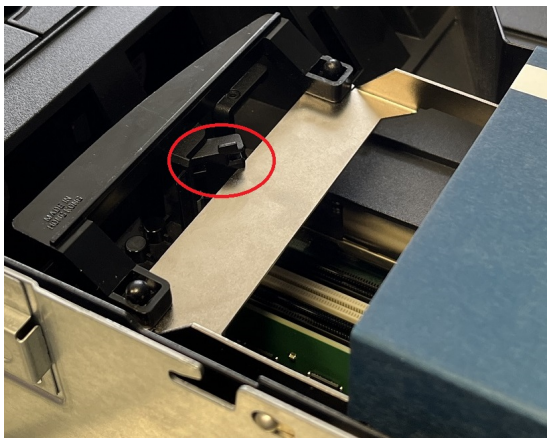


Figure 7 : Step 3+4) Secure System Clips, Collision

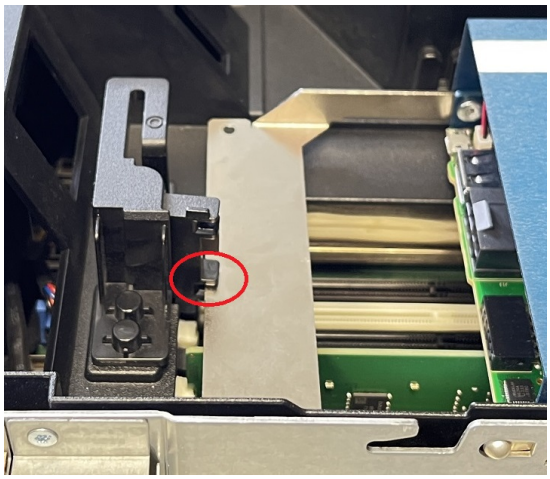


Figure 8 : Step 3+4) Secure System Clips, Correct

5 After the card has been installed and secured, the 8-pin ATX PCIe connector can be installed. This is required for application workloads using more than 65W of power. This cable should already be included with the host system, if not, please contact the host system supplier.

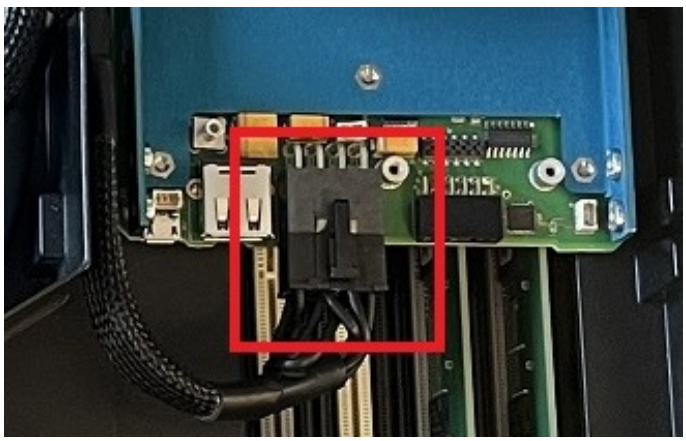


Figure 9 : Step 5) Plug in Power

2.3.4 Power Requirements

The ADM-PA120 draws power from the PCIe Edge and the 8-pin ATX power connector. The ADM-PA120 does not use or require the 3.3V power from the PCIe Edge (though it does use 3.3V AUX). To operate with PCIe edge only, ensure SW2-6 is OFF (see Switches). As per PCIe specification, users should limit the board power consumption to 66W when using only the PCIe edge power. Adding the 8-pin ATX connector provides additional 150W of power, bringing the total board power dissipation maximum to 216W.

It is possible to operate this product standalone with power from the 8-pin ATX power connector alone. Please be aware this reduces the total rated power of the card to 150W. Standalone operation requires a modified ATX power cable where the sense wires have been removed. Please contact **sales@alpha-data.com** to receive a modified ATX extension cable. When using a cable with the sense wires removed, ensure SW1-6 is set OFF which enables the 12V auto-detect feature. If SW2-6 is ON, the board will not power up unless both PCIe edge and the Aux cable are both used.

Power consumption estimation requires the use of the AMD XPE spreadsheet (www.xilinx.com/products/technology/power/xpe.html) and a power estimator tool available from Alpha Data. Please contact **support@alpha-data.com** to obtain this tool.

The power available to the rails calculated using XPE are as follows:

Voltage	Source Name	Current Capability
0.8	VCC_INT + VCC_IO + VCC_RAM + VCC_IO	120A
0.88	VCC_PMC + VCC_PSFP + VCC_PSLP+ VCC_CPM5	6A
0.92	MGTAVCC	10A
1.1	VCCO for LDDR4	8A
1.2	MGTAVTT	14A
1.5	GTY_AVCCAUX	1.2A
1.5	VCCO + VCCAUX + VCCAUX_PMC	8A
1.5	VCCO	8A
1.8	VCCO	1.2A
3.3	VCCO + QSFP	15A
5V	USB-A	0.5A

Table 3 : Available Power By Rail

2.4 Thermal Performance

If the ACAP core temperature exceeds 105 degrees Celsius, the ACAP design will be cleared to prevent the card from overheating.

The ADM-PA120 comes with a heat sink to avoid thermal overstress of ACAP, since it is typically the hottest point on the card. The ACAP die temperature must remain under 100 degrees Celsius. To estimate the ACAP die temperature: first take your total board power (see next paragraph), then multiply by Theta JA from the graph below, and add the resulting temperature to your system's internal ambient temperature.

The power dissipation can be estimated by using the Alpha Data power estimator in conjunction with the AMD Power Estimator (XPE) downloadable at www.xilinx.com/products/technology/power/xpe.html.

Power Estimation

- Download the Versal XPE or PDM tool.
- Set the device according to your part number details: Versal Premium Series, XCVP1202 or XCVP1502, VSVA2785 package, -2MS/-2HS speed grade, extended.
- Set the ambient temperature to your system ambient
- Select 'user override' for the effective theta JA. Then enter the figure associated with your system LFM in the blank field.
- Proceed to enter all applicable design elements and utilization in the following spreadsheet tabs
- Next acquire the PA120 power estimator from Alpha Data by contacting **support@alpha-data.com**.
- Enter the power figures from XPE, QSFP-DD (if used), and DRAM utilization into the Alpha Data spreadsheet to get a complete board-level estimate.

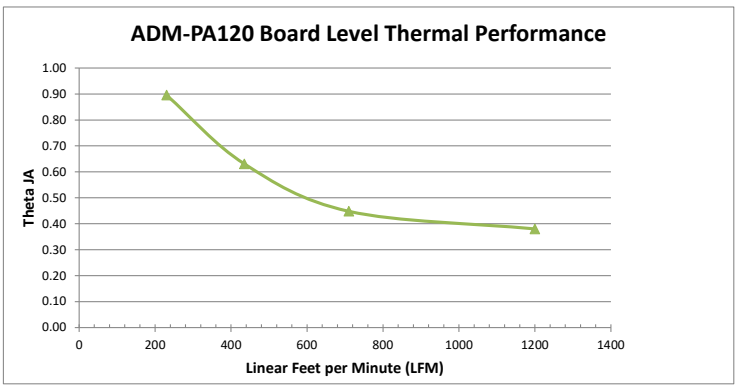


Figure 10 : Thermal Performance

2.5 Customizations

Alpha Data provides extensive customization options for existing commercial off-the-shelf (COTS) products. Some options include, but are not limited to: custom front panel interfaces, additional networking cages in adjacent slots, enhanced heat sinks, baffles, and circuit additions.

Please contact **sales@alpha-data.com** to get a quote and start your project today.

3 Functional Description

3.1 Overview

The ADM-PA120 is a high-performance reconfigurable computing card featuring the latest AMD Adaptive Compute Acceleration Platform (ACAP) platform with the Versal XCVP1202 or XCVP1502, three QSFP-DD interfaces, PCIe Gen4x16 or 2xGen5x8, four banks of LPDDR4 each 64 bits wide, GEM0 Ethernet, QSPI, uSD, USB, UART, a Digilent PMOD site, flexible front panel I/O (RS485 for ToD, 1PPS, 10MHz, and general purpose I/O), and a robust system monitor.

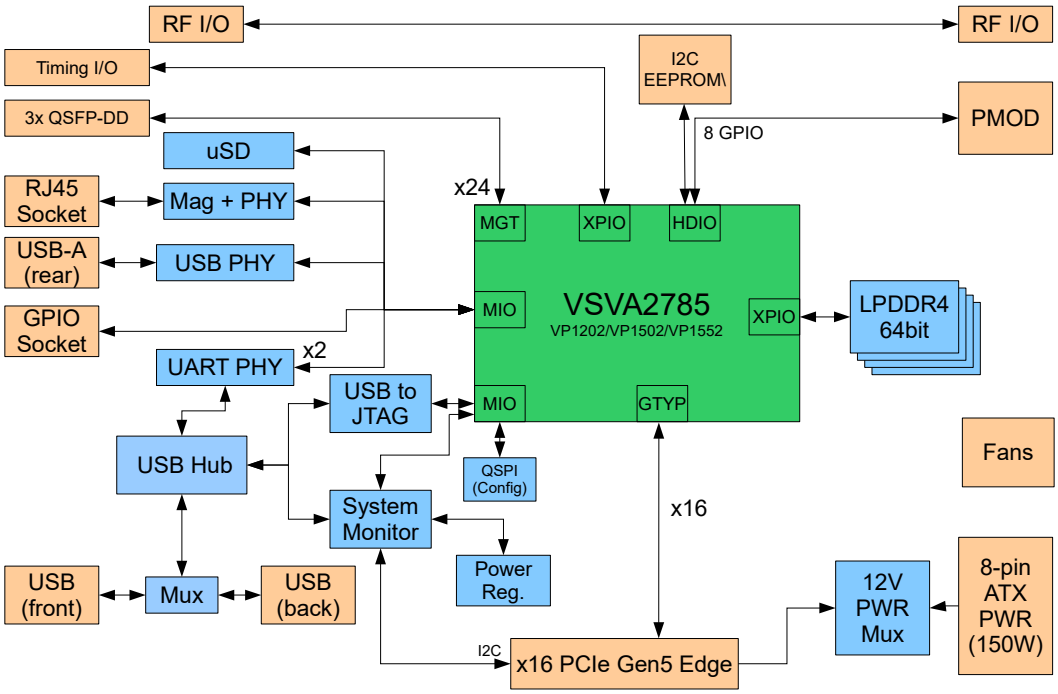


Figure 11 : ADM-PA120 Block Diagram

3.1.1 Switches

The ADM-PA120 has two octal DIP switches SW1 and SW2, located on the rear side of the board. The function of each switch is detailed below:

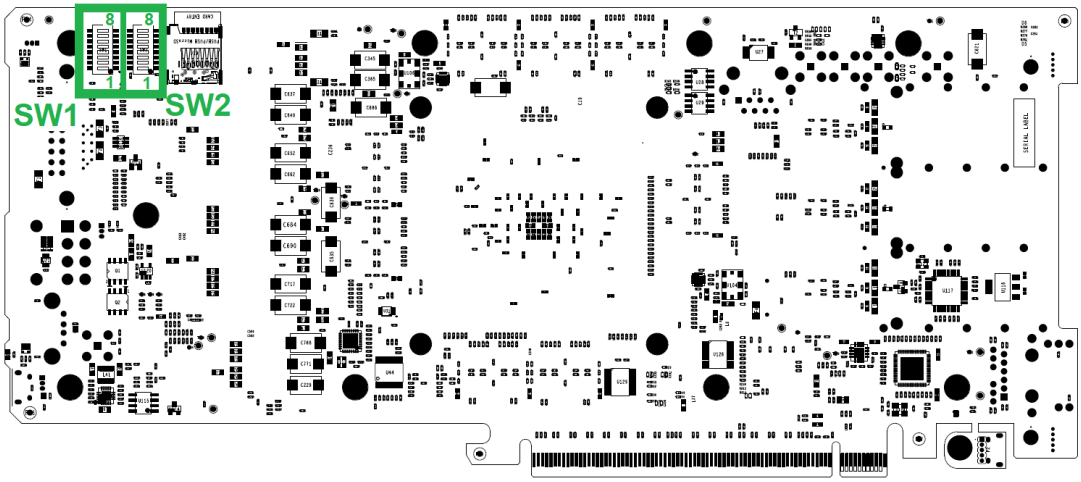


Figure 12 : Switches

Switch	Factory Default	Function	OFF State	ON State
SW1-1	OFF	Reserved	TBD	TBD
SW1-2	OFF	SI5402_I2C Isolate	Connect Si5402 I2C to PL	Isolate Si5402 I2C from PL
SW1-3	OFF	HOST_I2C_EN	System Monitor connected to PCIe slot I2C	System Monitor isolated from PCIe slot I2C
SW1-4	OFF	Service Mode	System Monitor normal operation	System Monitor Service Mode (firmware update etc.)
SW1-5	OFF	PERST to POR_B	PCIE RESET isolated from POR_B	PCIE RESET will drive POR_B low
SW1-6	OFF	POR_B	ACAP power on reset released	ACAP power on reset active
SW1-7	OFF	Reserved	TBD	TBD
SW1-7	OFF	Reserved	TBD	TBD
SW2-1	ON	BootMode 0	See Table 10	
SW2-2	OFF	BootMode 1	See Table 10	
SW2-3	OFF	BootMode 2	See Table 10	
SW2-4	OFF	BootMode 3	See Table 10	
SW2-5	OFF	Reserved	TBD	TBD
SW2-6	OFF	12V Auto-detect	12V auto-detect enabled	8-pin ATX cable and PCIe edge both required
SW2-7	OFF	Reserved	TBD	TBD
SW2-8	OFF	Power Off	Board will power up	Immediately power down

Table 4 : Switch Functions

3.1.2 LEDs

There are 10 LEDs on the ADM-PA120, 6 of which are general purpose and whose meaning can be defined by the user. The other 4 have fixed functions described below:

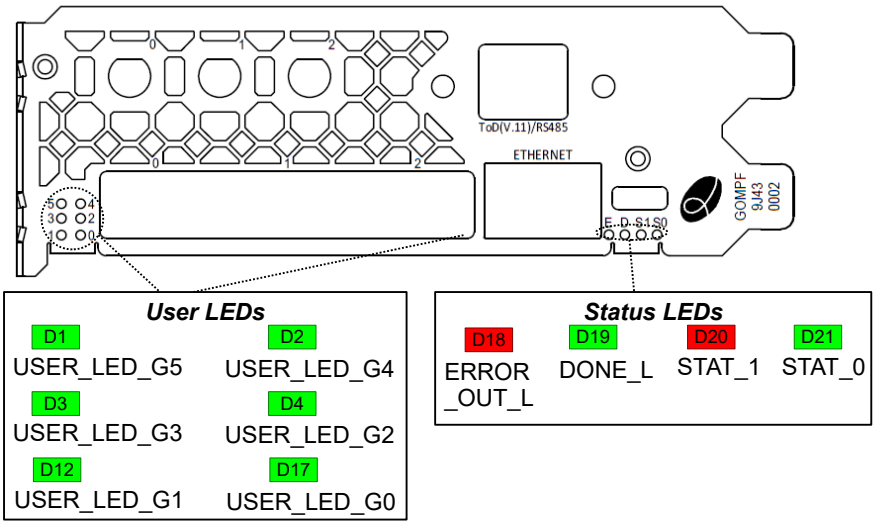


Figure 13 : Front Panel LEDs

Comp. Ref.	Function/Net Name	ON State	OFF State
D17	USER_LED_G0	User-defined '0'	User-defined '1'
D12	USER_LED_G1	User-defined '0'	User-defined '1'
D4	USER_LED_G2	User-defined '0'	User-defined '1'
D3	USER_LED_G3	User-defined '0'	User-defined '1'
D2	USER_LED_G4	User-defined '0'	User-defined '1'
D1	USER_LED_G5	User-defined '0'	User-defined '1'
D18	ERROR_OUT_L	Boot error	No error reported
D19	DONE_L	PL is configured	PL is not configured
D20	Status 1	See Status LED Definitions	
D21	Status 0	See Status LED Definitions	

Table 5 : LED Details

See Section Complete Pinout Table for full list of user controlled LED nets and pins

3.2 Clocking

The ADM-PA120 provides flexible reference clock solutions for the many multi-gigabit transceiver quads, LPDDR4 banks, and PL fabric. The reprogrammable clocks from the LMK61E2 are reconfigurable from the front panel Micro USB Interface by using Alpha Data's avr2util utility. This allows the user to configure almost any arbitrary clock frequency during application run time. The maximum clock frequency for the LMK61e2 is 900MHz. Customers who purchase RD-PA120 also have the option of embedding IP into their ACAP design that permits programmable clock reconfiguration via PCIe or from within the ACAP.

There is one Si5344 jitter attenuator. This can provide clean and synchronous clocks to the QSFP-DD quad locations at many clock frequencies. The Si5344 can be reconfigured over I2C using a controller embedded in the FPGA design.

There is one Si5402 Network Synchronizer. This can provide synchronous clocks for 5G, SyncE, and IEEE 1588 applications with 10Mhz and 1PPS inputs. The Si5402 can be reconfigured over I2C using a controller embedded in the FPGA design. Using this chip requires support directly from Skyworks. Alpha Data does not support application software for this device.

All clock names in the section below can be found in Complete Pinout Table.

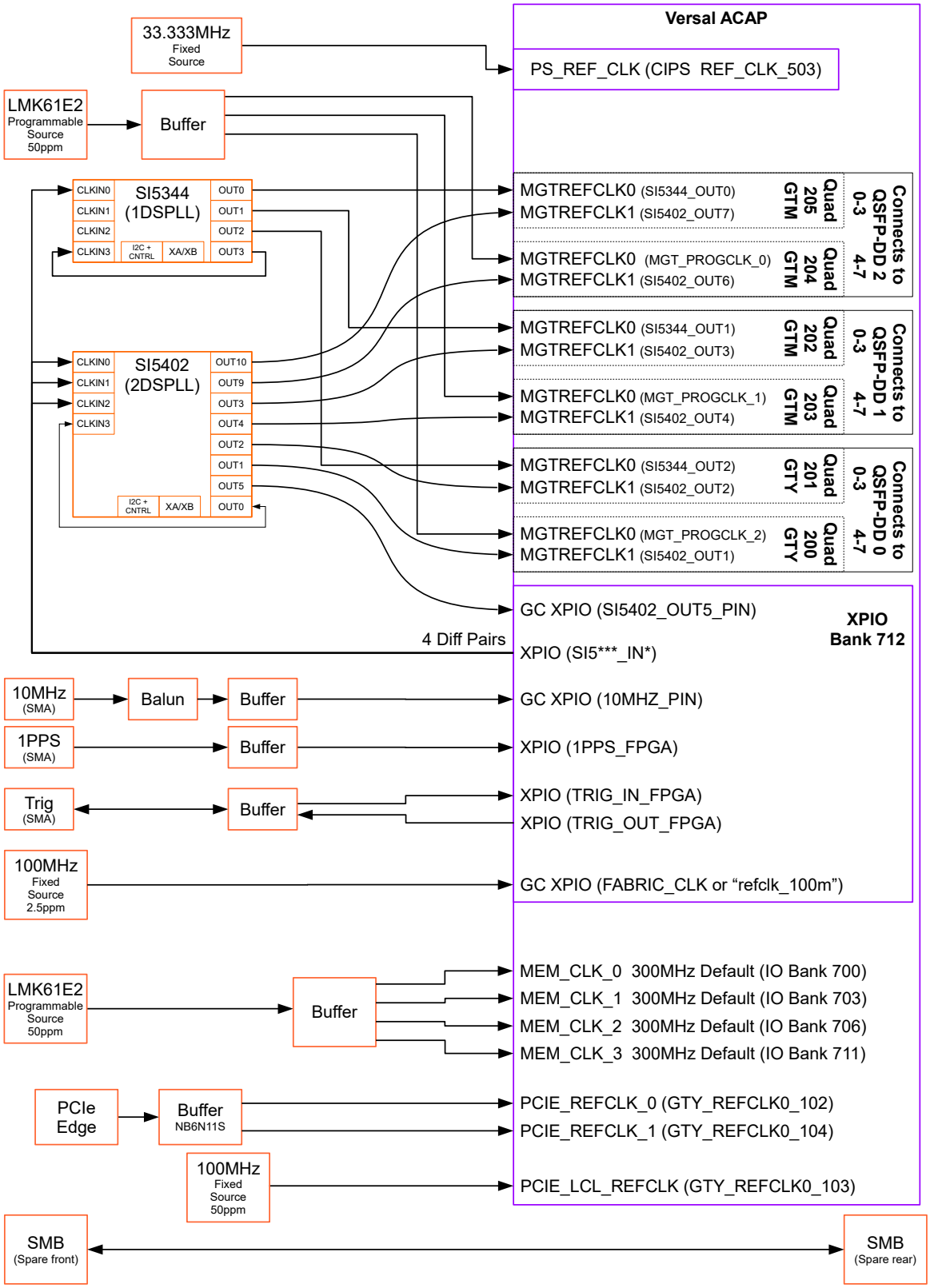


Figure 14 : Clock Topology

3.2.1 LMK61E2

The ADM-PA120 uses the LMK61E2 for arbitrary clock frequency synthesis. For complete technical details, please reference the datasheet:
https://www.ti.com/lit/ds/symlink/lmk61e2.pdf

The ADM-PA120 uses two LMK61E2 devices in the clock architecture. These can be accessed through either the USB or PCIe link using the AVR2UTIL application. See additional details on avr2util in the section: Micro USB Interface.

To re-program the LMK61E2 in a non-volatile manner, issue the following command:

```
avr2util <other options> setclknv-regmap <clock#> <reg. map file>
```

> **Note:**
> Each LMK61E2 is rated for only 100 non-volatile write operations.

To re-program the LMK61E2 in a volatile manner, issue the following command:

```
avr2util <other options> setclk-regmap <clock#> <reg. map file>
```

<other options> should be left blank for PCIE, and '-usbcom' for USB.

<clock#> is 0 for MGT_PROGCLK and 1 for MEM_CLK.

<reg. map file> is a text file generated using the "LMK61xx Oscillator Programming Tool — SNAC074.ZIP" which can be obtained with a TI login from this page: https://www.ti.com/tool/LMK61E2EVM. After you have the tool installed, launch the application, type in the desired frequency, select "LVDS" output standard, click "Generate Configuration", then go to "File->Export hex register values"

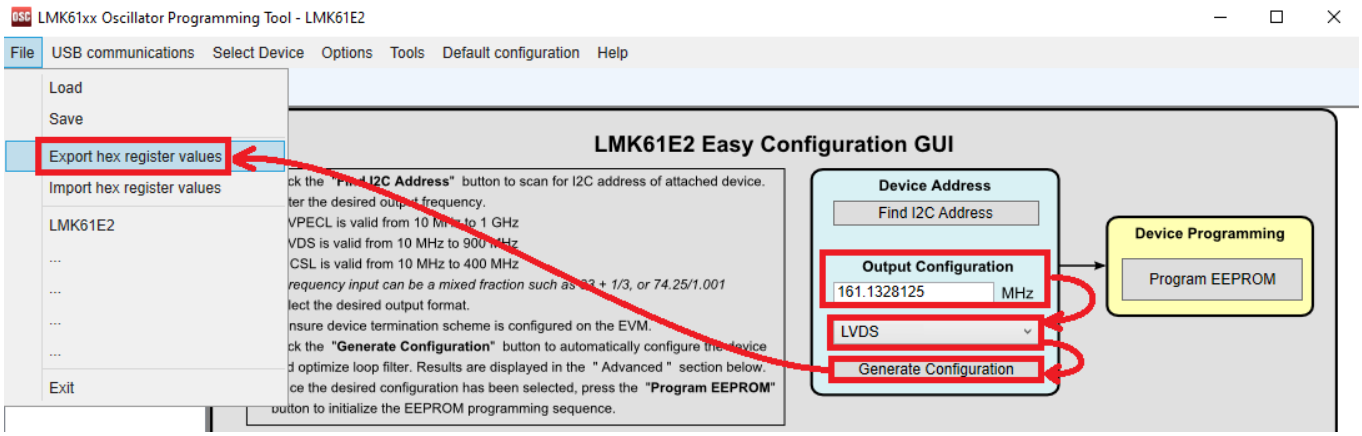


Figure 15 : LMK61xx Oscillator Programming Tool GUI

3.2.2 Si5344

If jitter attenuation is required please see the SI5344 datasheet.

The SI5344 is pre-configured to expect 322.265625MHz on IN0, and will output 161.1328125MHz on all outputs. The non-volatile memory on the device can be changed one more time. For details on burning the non-volatile memory, see section “4.3 NVM Programming” of the SI5344 Reference Manual.

There is one input clock that originates in the ACAP PL (board net name SI5344_IN0_P/N). This allows the application design to feed the clock from anywhere within the ACAP PL.

Three output clocks are connected to quads 201, 202, and 205 to provide clocking capability for each QSFP-DD interface.

The LOL signals for the Si5344 are available for use, and can be located at net names SI5344_LOL_XAXB_1V5_N and SI5344_LOL_1V5_N in the Complete Pinout Table.

The active low reset of the Si5344 is accessible to the ACAP. See net names SI5344_RST_1V5_N in the Complete Pinout Table.

Note:
Each sideband signal has an external pull-up resistor.

The Si5344 configuration register map is volatile unless burned into NVM. You are only allowed to burn a register map twice during the product's lifetime, and Alpha Data has used one of these already. To write the register map use nets SI5344_SDA_1V5 and SI5344_SCL_1V5 at pins located in the Complete Pinout Table. The Si5344 device is configured using the I2C address shown in the table below:

device	7bit Hex Address	Binary Address
Si5344	68	110_1000

Table 6 : Si5344 address table

3.2.3 Si5402

If a Network Synchronizer Clock for 5G/SyncE/IEEE 1588 applications is required please see the reference documentation for the Si5402.
https://www.skyworksinc.com/en/Products/Timing/NetSync-Network-Synchronizer-Clocks/Si5402A
Contact skyworks directly for detailed support and to set up an NDA:
https://www.skyworksinc.com/Talk-To-Sales

There are three input clocks that originate in the ACAP PL (board net name SI5402_IN*_P/N). This allows the application design to feed the clock from anywhere within the ACAP PL and forward 10MHz and 1PPs signals.

Six output clocks are connected to quads 200 through 205 to provide clocking capability for each QSFP-DD interface.

The GPIO signals for the Si5402 are available for use and can be located at net names SI5402_GPIO* in the Complete Pinout Table.

The active low reset of the Si5402 is accessible to the ACAP. See net names SI5402_RST_1V5_N in the Complete Pinout Table.

Note:
Each sideband signal has an external pull-up resistor.

The Si5402 configuration register map is volatile. To write the register map use nets SI5402_1V5_SDA and SI5402_1V5_SCL at pins located in the Complete Pinout Table. The Si5402 device is configured using the I2C address shown in the table below:

device	7bit Hex Address	Binary Address
Si5402	58	101_1000

Table 7 : Si5402 address table

3.2.4 PCIe Reference Clocks

The 16 MGT lanes connected to the PCIe card edge use MGT tiles 102 through 105 and use the host system's 100 MHz PCIe reference clock (net name PCIE_REFCLK_0_P/N or PCIE_REFCLK_1_P/N in the Complete Pinout Table).

Alternatively, a more stable but asynchronous onboard 100MHz clock is available as well (net name PCIE_LCL_REFCLK_P/N in the Complete Pinout Table).

3.2.5 Fabric Clock

The design offers a fabric clock (net name FABRIC_CLK_P/N) which is a high accuracy 2.5ppm 100 MHz clock. This clock is intended to be used for the PL designs. The fabric clock is connected to a Global Clock (GC) pin.

Use constraints IOSTANDARD LVCMOS15 for this reference clock.

See net names FABRIC_CLK_1V5 in the Complete Pinout Table for pin locations.

In the Alpha Data provided board file, this is called "refclk_100m"

3.2.6 PS Reference Clock (PS_REF_CLK)

A 33.333MHz clock is fed into the dedicated REF_CLK_503 pin to drive the processor system. This clock has an accuracy tolerance of 50ppm.

3.2.7 MGT Programable Clock

The MGT reference clock connects to one quad of each QSFP-DD connector. This programable clock has a default 161.1328125MHz reference clock. This clock frequency can be changed to any arbitrary clock frequency up to 900MHz by re-programming the LMK61E2 reprogrammable clock oscillator. See details on avr2util in the section: Micro USB Interface.

See net names MGT_PROGCLK_*_PIN_P/N in the Complete Pinout Table for pin locations.

3.2.8 Memory Clocks

Each of the four memory banks has their own buffered 300MHz reference clock. This clock frequency can be changed to any arbitrary clock frequency up to 900MHz by re-programming the LMK61E2 reprogrammable clock oscillator. See details on avr2util in the section: Micro USB Interface.

See net names MEM_CLK_*_PIN_P/N in the Complete Pinout Table for pin locations.

See LPDDR4 SDRAM for more information on the memory banks and their physical locations.

These clocks are not fabric accessible. They are reserved for the Versal LPDDR4 cores.

3.3 PCI Express

The ADM-PA120 is capable of PCIe Gen 1/2/3/4 with 1/4/8/16 lanes and bifurcated Gen 5 with 1/4/8 lanes. The ACAP drives these lanes directly using the Integrated PCI Express block from AMD. Negotiation of PCIe link speed and number of lanes is generally automatic and does not require user intervention.

PCI Express reset (PERST#) is connected to the ACAP through a buffer. See Complete Pinout Table signal PERST_PL_L for fabric accessible location, and PCIE_RST_1V8_L for the PS locations.

The pin assignments for the high-speed lanes are provided in the pinout attached to the Complete Pinout Table, see net names PCIE_TX*_PIN_P/N and PCIE_RX*_P/N.

3.4 LPDDR4 SDRAM

Two banks of LPDDR4 SDRAM memory are soldered down to the board. The available density of the memory is 4GB/per bank, 16GB total. The memory interface is 64-bit wide data. The maximum signalling rate is 3900 MT/s for banks 0-2 and 3200MT/s for bank 3. This speed limitation is a limitation of the ACAP device, see AMD specifications for more details.

Memory solutions are available from AMD (See AMD PG313 Versal ACAP Programmable Network on Chip and Integrated Memory Controller v1.0). LPDDR4_0 through 2 use the Non-Flipped Pinout, and LPDDR4_3 uses the Flipped Pinout. An example memory exerciser project is included in the RD-PA120. All pin location information is included in Complete Pinout Table and the board file.

The components used are Micron MT53E512M32D1ZW-046 IT or equivalent.

Note:
For customers using the /C1 version of this product, the LPDDR4 pinout is slightly different. Please contact support@alpha-data.com if you need additional details.

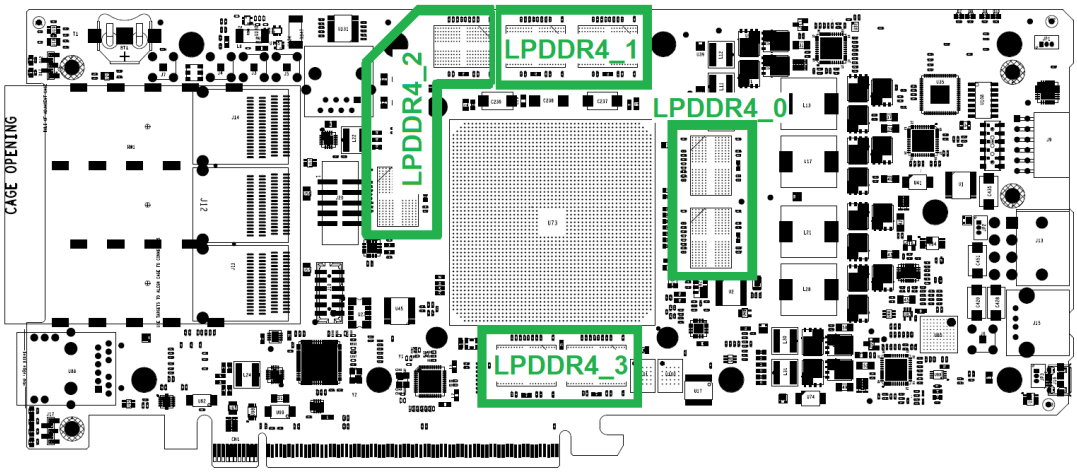


Figure 16 : LPDDR4 bank locations by index

3.5 QSFP-DD

Three QSFP-DD cages are available at the front panel. These cages are capable of housing either QSFP28 or QSFP-DD cables (backwards compatible). Both active optical and passive copper QSFP-DD/QSFP28 compatible models are fully compliant. The communication interface can run at up to 28 Gbps per channel on GTY and 56 Gbps per channel on GTM. Two cages connect to GTM transceivers and one cage connects to GTY transceivers. Each QSFP-DD cage has 8 channels. This cage is ideally suited for 8x 10G/25G/50G, 2x 100G/200G, 1x400G Ethernet, or any other protocol supported by the Xilinx GTY Transceivers. Please see AMD User Guide AM002 (GTY) and AM017 (GTM) for more details on the capabilities of the transceivers.

All QSFP-DD cages have control signals connected to the FPGA. Their connectivity is detailed in the Complete Pinout Table at the end of this document. The notation used in the pin assignments is QSFP0*, QSFP1*, and QSFP2*, with locations clarified in the diagram below.

The Management Interface of each QSFP-DD cage is connected to the ACAP, as detailed in Complete Pinout Table. The available signals are SDA/SCL (I2C), INT_L (interrupt), LPMODE (low power mode), RST_L (reset), and MODPRS_L (module present).

Note:
The LPMODE (Low Power Mode) to the cage is pulled down by default.

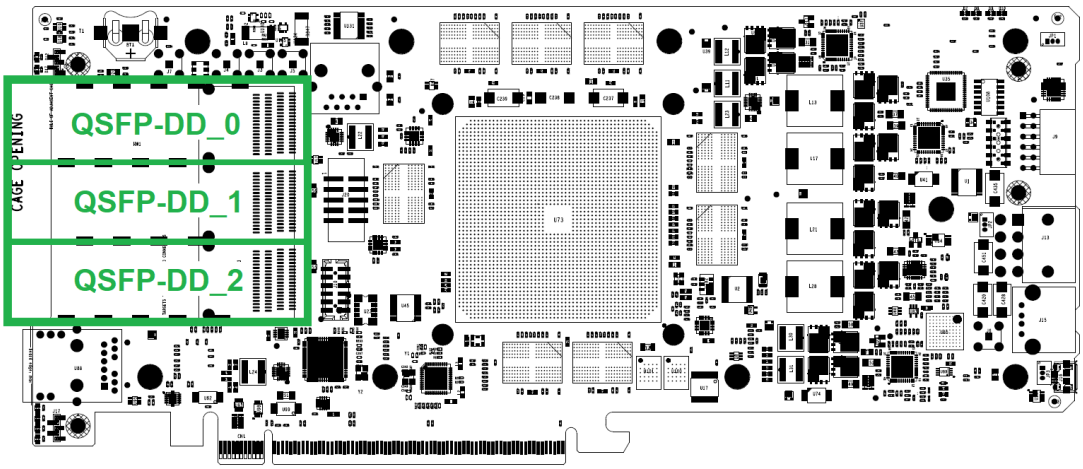


Figure 17 : QSFP-DD Location

3.6 Front I/O timing inputs

The ADM-PA120 includes several timing and signal inputs that are critical for high-performance synchronous networking. This section details the four available timing inputs.

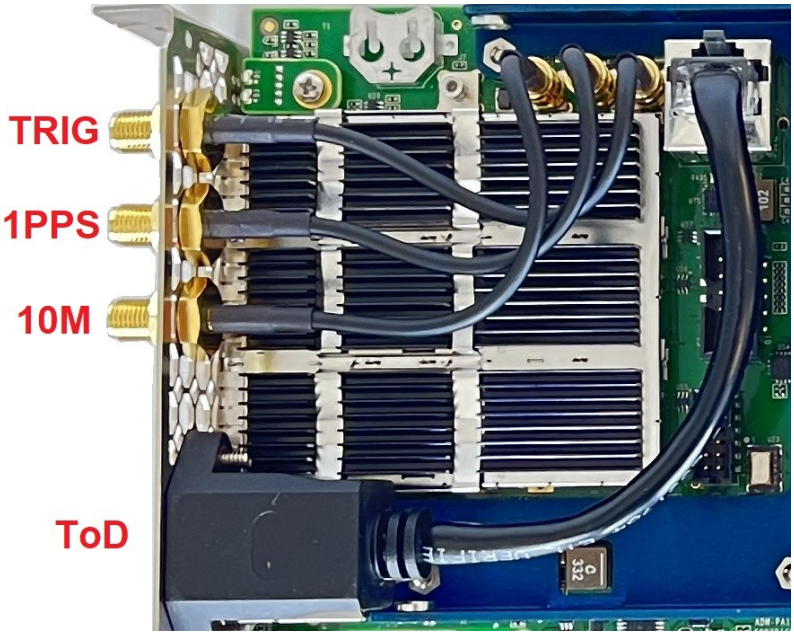


Figure 18 : Front I/O timing inputs

3.6.1 Trigger Input/Output (I/O)

One of the SMA connectors is used for a general purpose I/O. This signal can be driven as an output or received as an input.

A small '0' is printed on the faceplate at the TRIG I/O connector.

The input receiver is always active. The output driver buffers net "TRIG_OUT" onto the SMA connector when net "TRIG_OUT_EN" is driven low.

The trigger input is designed for unbalanced 50-ohm input signal at either 5V or 1.8V signal levels. The port is configured as an input when both nets "TRIG_TE_EN" and "TRIG_OUT_EN" are driven high. "TRIG_TE_EN" actives a 50-ohm load to GND. "TRIG_OUT_EN" is an active low control signal that disables the output driver when driven high.

The buffers used are low latency (less than 5ns), and the full schematic detail is shown below:

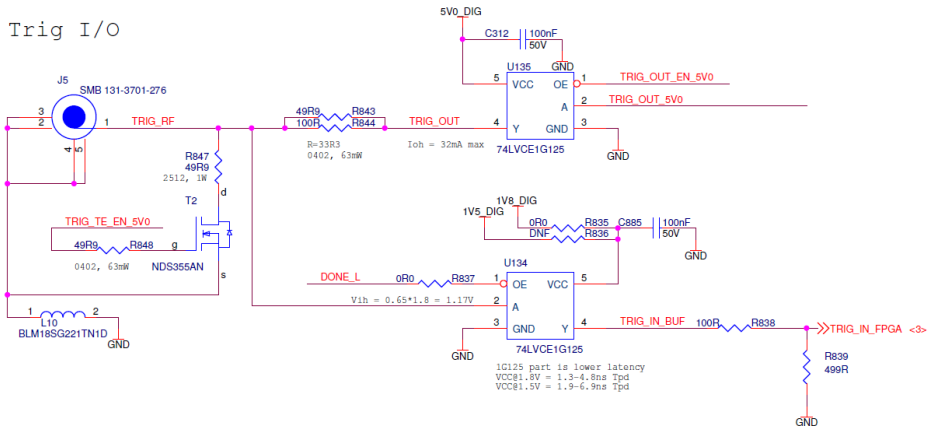


Figure 19 : Trig Schematic

3.6.2 1PPS Input

One of the SMA connectors is used for a 1PPS input. This is a general input that can be used for many unbalanced 50-ohm input signal up to 5V in amplitude.

A small '1' is printed on the faceplate of the 1PPS input connector.

The buffers used are low latency (less than 5ns), and the full schematic detail is shown below:

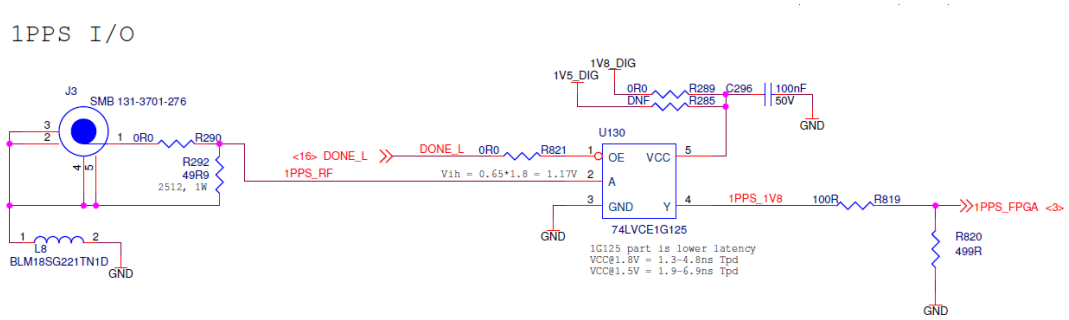


Figure 20 : 1PPS Input Schematic

3.6.3 10MHz Input

One of the SMA connectors is used for a 10MHz input. This is a specific input that has a narrow frequency band around 10MHz and expects 0.5V to 5V peak-to-peak input voltage.

A small '2' is printed on the faceplate at the 10MHz input connector.

The signal passes through a balun and LVDS buffer before entering the ACAP. The full schematic detail is shown below:

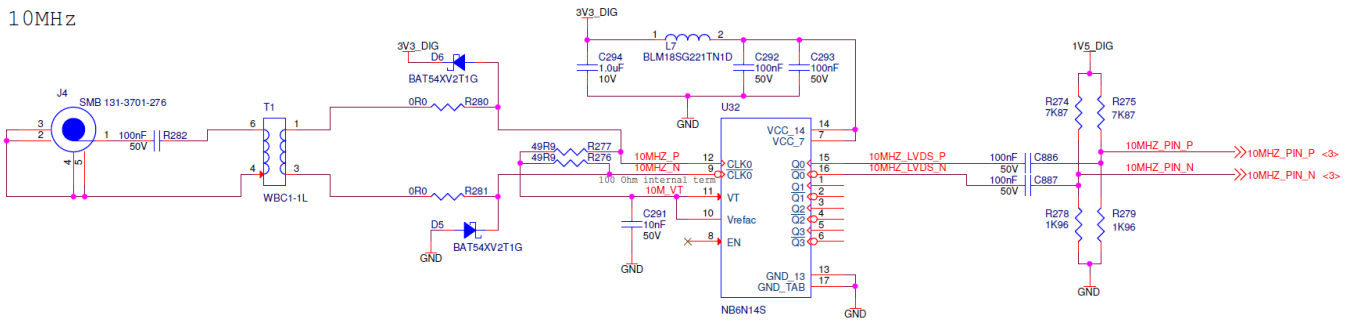


Figure 21 : 10MHz Input Schematic

3.6.4 Time of Day (ToD) / One Pulse per Second (1PPS)

One of the RJ45 jacks at the front panel is for Time of Day (ToD) or generic RS485 input/output. The port is labeled on the front panel for clarity.

Net "485_?_DE/RE_L_FPGA" is used to control the direction of this interface. By default, the DE/RE_L pins are pull-down, so the RS485 drivers are set as inputs to the ACAP. If either DE/RE_L pins are driven high, the RS485 transceivers will become outputs respectively.

The transceivers are low latency (18.5ns ±3.5ns), and the full schematic detail is shown below:

TOD + 1PPS

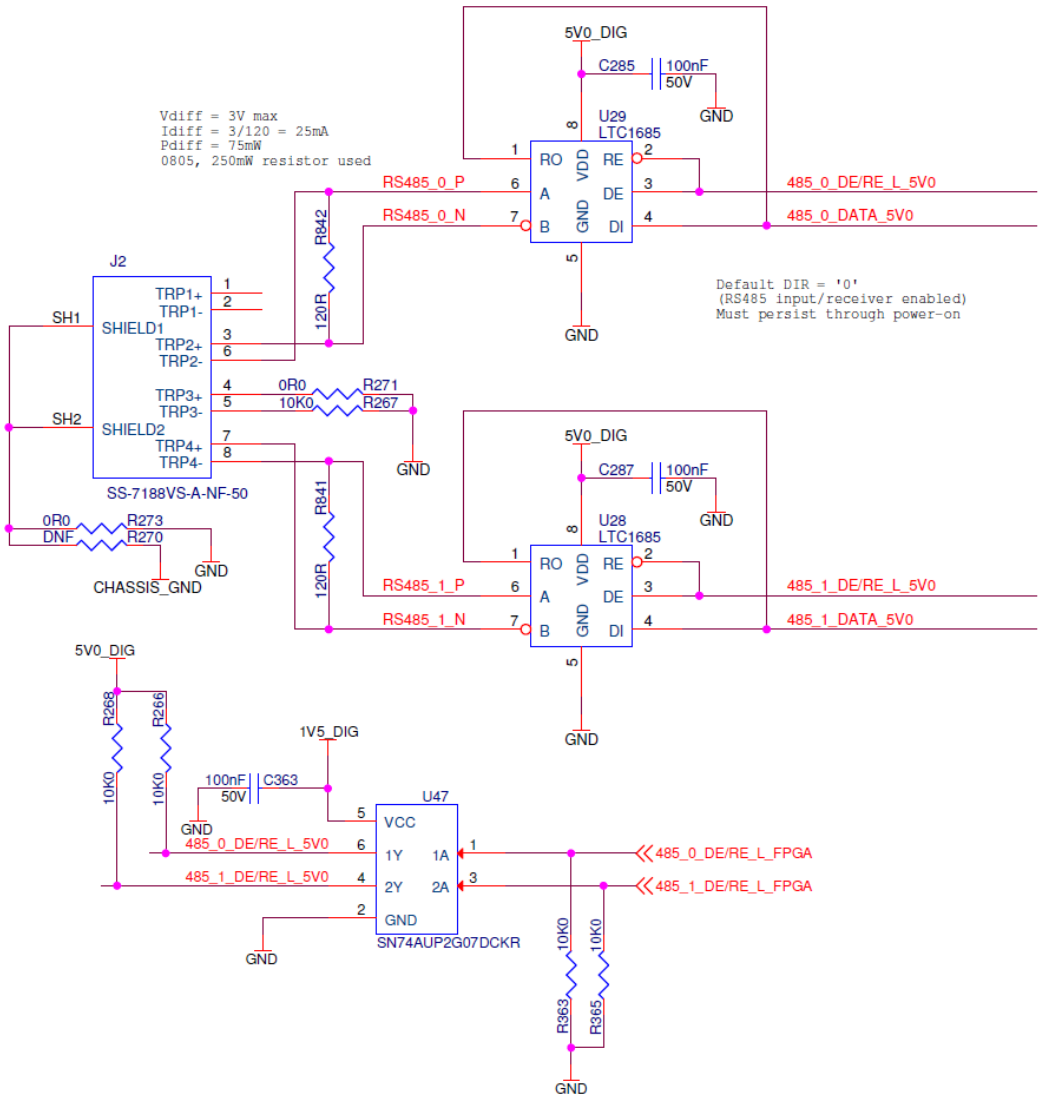


Figure 22 : ToD/1PPS or RS485 Schematic

3.7 System Monitor

The ADM-PA120 monitors select temperatures, voltages, and currents in order to provide an indication of board health. The monitoring is implemented using an AVR microcontroller. This information can be read out via USB using the avr2util utility. Alternatively, the sensor information can be read directly by the ACAP or via PCIe if RD-PA120 is purchased (reference design package).

If the core ACAP temperature exceeds 105 degrees Celsius, the ACAP image will be cleared to prevent damage to the card.

Monitors	Identifier	Purpose/Description
ETC	ETC	Elapsed time counter (seconds)
EC	EC	Event counter (power cycles)
12V_AUX	ADC00	12V board input voltage from 8-pin ATX cable
12V_AUX_I	ADC01	12V board input current from 8-pin ATX cable in amps
12V_EDGE	ADC02	12V board input voltage from PCIe Edge
12V_EDGE_I	ADC03	12V board input current from PCIe Edge in amps
3V3_AUX	ADC04	3.3V auxiliary board input supply from PCIE edge
3V3_DIG	ADC05	3.3V generated onboard for QSFP-DD and other circuits
1V8_SI5402	ADC06	1.8V generated onboard for Si5402
1V5_DIG	ADC07	1.5V generated onboard for ACAP IO voltage (VCCO)
1V5_AVCCAUX	ADC08	1.5V generated onboard for ACAP Aux voltage
1V2_AVTT	ADC09	1.2V generated onboard for transceiver Power (AVTT)
1V1_DIG	ADC10	1.1V generated onboard for LPDDR4 SDRAM and ACAP (VCCO)
0V92_AVCC	ADC11	0.88V generated onboard for transceiver Power (AVCC)
VCC_IPMC	ADC12	0.88V generated onboard for ACAP core
VCC_INT	ADC12	0.8V generated onboard for ACAP core
uC_Temp	TMP00	uC on-die temperature
Board0_Temp	TMP01	Board temperature at U58
Board1_Temp	TMP02	Board temperature at U80
ACAP_Temp	TMP03	ACAP on-die temperature

Table 8 : Voltage, Current, and Temperature Monitors

3.7.1 System Monitor Status LEDs

LEDs D20 (Red) and D21 (Green) indicate the card health status.

LEDs	*Status*
Green	Running and no alarms
Green + Red	Standby (Powered off)
Flashing Green + Flashing Red (together)	Attention - critical alarm active
Flashing Green + Flashing Red (alternating)	Service Mode
Flashing Green + Red	Attention - alarm active
Red	Missing application firmware or invalid firmware
Flashing Red	ACAP configuration cleared to protect board

Table 9 : Status LED Definitions

3.8 Micro USB Interface

The ACAP can be configured directly from the USB connection on either the front panel or the rear card edge. The ADM-PA120 utilizes the Digilent USB-JTAG converter which is supported by the AMD software tool suite. Simply connect a micro-USB AB-type cable between the ADM-PA120 USB port and a host computer with Vivado installed. Vivado Hardware Manager will automatically recognize the ACAP and allow you to configure the ACAP and the SPI configuration Flash memory.

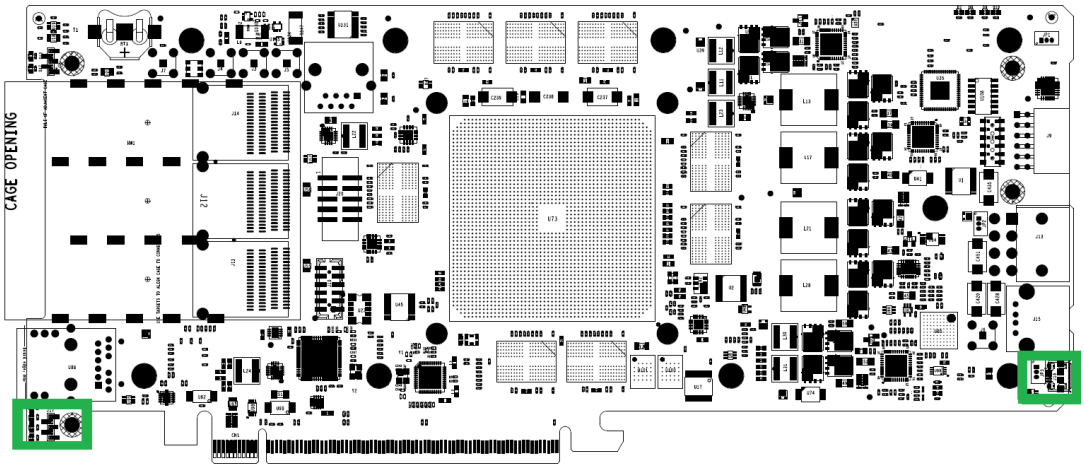


Figure 23 : USB Location

The same USB connector is used to directly access the system monitor system. All voltages, currents, temperatures, and non-volatile clock configuration settings can be accessed using Alpha Data's avr2util software at this interface.

Avr2util for Windows and the associated USB driver is downloadable here:
https://support.alpha-data.com/pub/firmware/utilities/windows/

Avr2util for Linux is downloadable here:
https://support.alpha-data.com/pub/firmware/utilities/linux/

Use this command to see all options:

```
avr2util.exe /?
```

Use this command to display all sensor values:

```
avr2util.exe /usbcom \\.\com4 display-sensors
```

Here is an example of changing the MGT_PROGCLK to 156.25MHz immediately:

```
avr2util.exe /usbcom \\.\com4 setclk-regmap 0 lmk61e2_lvds_156250000.txt
```

To generate the register text file, please reference LMK61E2.

Setclk index 0 = MGT_PROGCLK and index 1 = MEM_CLK.

Here is an example of changing the boot mode from uSD to QSPI on the next power-up event:

```
avr2util.exe /usbcom \\.\com4 set-boot-mode qspi24
```

Boot-mode commands use open drain drivers and can only drive mode pins low.

In the examples above, change 'com4' to match the com port number assigned under Windows Device Manager.

3.9 Configuration

There are three main ways of configuring the ACAP on the ADM-PA120:

- From QSPI Flash memory, at power-on, as described in Section 3.9.1
- From uSD Flash memory, at power-on, as described in Section 3.9.2
- Using USB cable connected at either USB port as described in Section 3.9.3

3.9.1 Configuration From QSPI Flash Memory

The ACAP can be automatically configured at power-on from two 1 Gbit QSPI flash memory devices configured as an x8 dual parallel SPI device (2x Micron part number MT25QU01GCBB8E12).

The ADM-PA120 is shipped with a simple "hello world" application that prints text on UART0 loaded into QSPI. On request, Alpha Data can pre-load custom bitstreams during the production test. Please contact **sales@alpha-data.com** in order to discuss this possibility.

At power-on, the ACAP attempts to configure itself automatically according to the mode pins as described in Section 3.9.4. If the mode is set to QSPI24 or QSPI32, the ACAP will search on the header of the binary that has been flashed into the card. This normally results in SPIx8 configuration.

The Alpha Data System Monitor is also capable of reconfiguring the flash memory and reprogramming the ACAP. This provides a useful failsafe mechanism to re-program the ACAP even if it drops off the PCIe bus. The system monitor can be accessed with avr2util over USB at the front panel and rear edge.

3.9.2 Configuration From uSD Flash Memory

The ACAP can be automatically configured at power-on from the Micro Secure Digital card (uSD) slot along the north edge of the card.

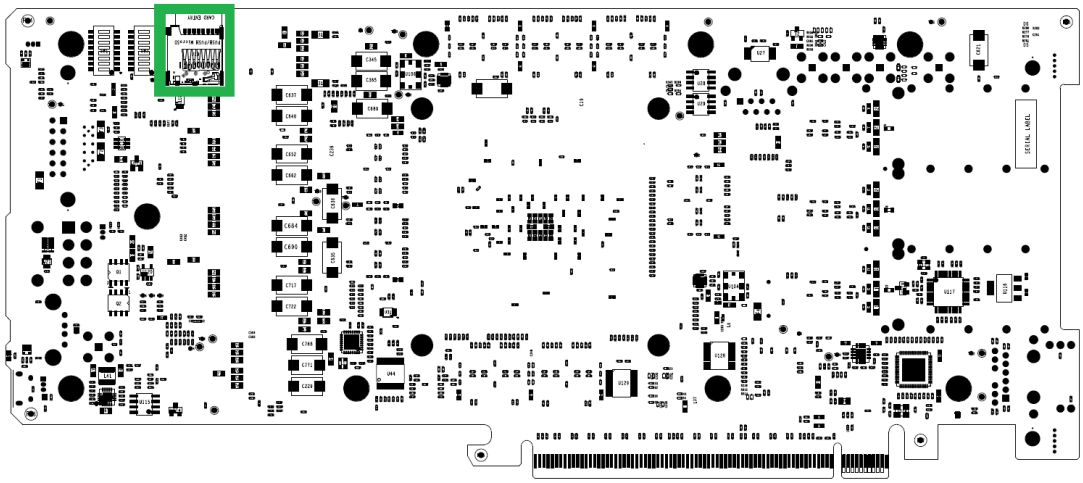


Figure 24 : uSD Location

The ADM-PA120 is shipped with a simple PCIe endpoint bitstream which should be visible to the operating system (using Windows Device Manager or “lspci” in Linux) in order to provide confidence that the card is working correctly when installed in a system. On request, Alpha Data can pre-load custom bitstreams during the production test. Please contact **sales@alpha-data.com** in order to discuss this possibility.

At power-on, the ACAP attempts to configure itself automatically according to the mode pins as described in Section 3.9.4. Alpha Data ships these cards set to the uSD boot mode by default.

3.9.3 Configuration via JTAG

A micro-USB AB Cable may be attached to the front panel or rear edge USB port. This permits the ACAP to be reconfigured using the AMD Vivado Hardware Manager and Vitis via the integrated Digilent JTAG converter box. The device will be automatically recognized in Vivado Hardware Manager and Vitis.

For more detailed instructions, please see “Using a Vivado Hardware Manager to Program an FPGA Device” section of AMD UG908

3.9.4 Boot Modes

MODE3 (SW2-4)	MODE2 (SW2-3)	MODE1 (SW2-2)	MODE0 (SW2-1)	Boot Mode
ON	ON	ON	ON	JTAG
ON	ON	ON	OFF	Quad SPI (24-bit addressing)
ON	ON	OFF	ON	Quad SPI (32-bit addressing)
OFF	OFF	OFF	ON	SD Flash - SD 3.0

Table 10 : Boot Mode Selection

Note: all other possible switch settings are reserved / invalid.

The system monitor can also control the mode pins, enabling remote changes to boot the device for golden image fallback and recovery. The system monitor can drive the MODE pins low (open drain drive), so it is recommended to leave the switches in the OFF positions or set them to SD 3.0 boot mode. From there, the user can issue commands to change the boot mode between "sd1_v3" or "qspi32" and then reboot the board:
Loading an image from qspi32 remotely:

- avr2util.exe -usbcom com4 set-boot-mode qspi32
- avr2util.exe -usbcom com4 set-brd-power off
- avr2util.exe -usbcom com4 set-brd-power on

Use set-boot-mode to immediately change boot mode settings. Use set-boot-mode-nv to change boot mode setting in a non-volatile manner after a complete system power cycle.

3.10 ULPI USB Interface

The MIO ULPI USB interface is instantiated. See MIO Map

Part number USB3320C-EZK is used for PHY electrical conversion. This PHY is capable of USB 2.0 communication speeds. An onboard supply provides 5V @ 500mA on the VBUS pin of the USB receptacle. The location of the USB PHY is located along the back edge of the card.

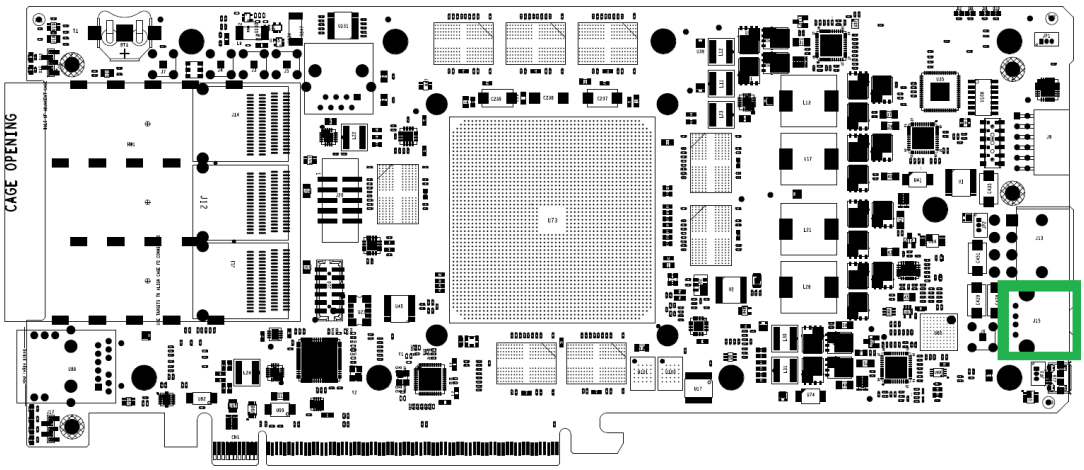


Figure 25 : ULPI USB Location

3.11 UART interfaces

UART0 and UART1 interfaces are available. See MIO Map

Both of these UART interfaces are brought out through the onboard USB hub which can be accessed at either the front or the back edge of the card.

UART0 passes through an FT230XQ USB to UART converter. This device is powered from the USB VBUS supply provided by the USB cable. This UART interface will appear in the host system as soon as the USB cable is installed, even before the ADM-PA120 is powered up. This interface is suitable for capturing power-on messages from the processor.

UART1 passes through an FT2232HQ USB to UART converter. This is the same IC that performs the USB to JTAG conversion. This UART interface will not appear in the system until after the board is fully powered and is not suitable for capturing power-on messages from the processor.

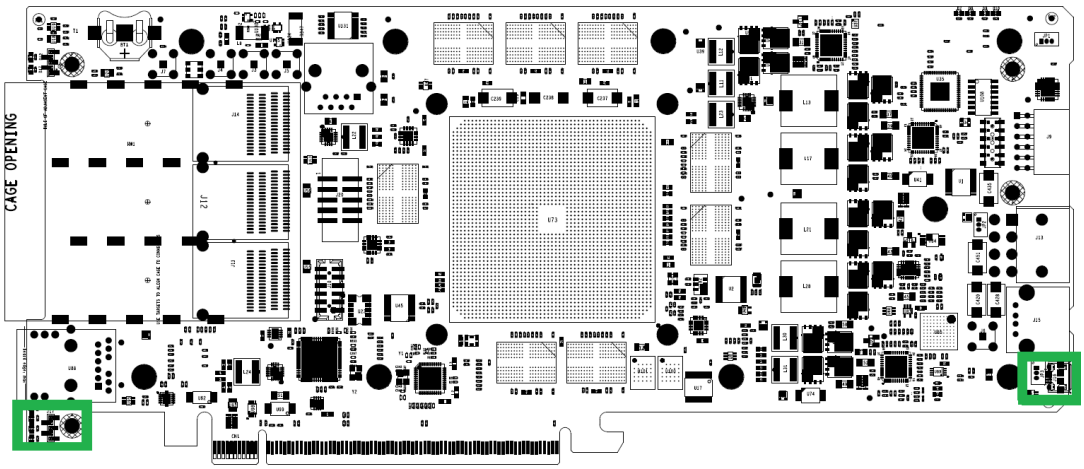


Figure 26 : USB UART Location

3.12 GEM0

The Gigabit Ethernet Manager (GEM0) is interfaced with a Microchip VSC8541 to provide 10/100/1000 Base-T Ethernet to the ACAP. This interface is accessible at the front panel.

A dedicated reset signal is connected to the MIO pins, see signal name GEM0_RST_L in Complete Pinout Table. This pin has an external pull-up and its use is optional.

See MIO Map

The Ethernet jack has two LED colors available. They are mapped to the VSC8541 PHY LED[*] pins and their function is user-defined over the GEM0_MDIO interface. The LED mapping is: green->LED[0], orange->LED[1]

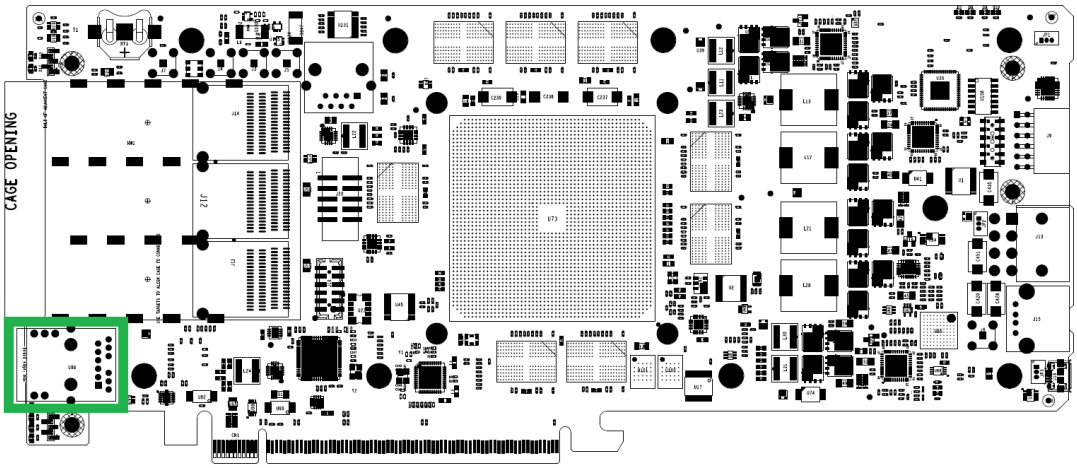


Figure 27 : GEM0 Ethernet Location

3.13 User EEPROM

A 2Kb I2C user EEPROM is provided for storing MAC addresses or other user information. The EEPROM is part number CAT34C02HU4IGT4A

The address pins A2, A1, and A0 are all strapped to a logical '0'.

Write protect (WP), Serial Clock (SCL), and Serial Data (SDA) pin assignments can be found in Complete Pinout Table with the names SPARE_WP, SI5344_SDA_1V5, and SI5344_SCL_1V5 respectively.

WP, SDA, and SCL signals all have external pull-up resistors on the card.

3.14 PMOD

The ADM-PA120 includes a twelve-pin right-angle connector PMOD host interface at the rear edge of the card with a full 0.9" clearance. This interface is connected to the PL of the ACAP.

See the PMOD Specification for full details.

Signals from this interface start with the name PMOD* and can be found in Complete Pinout Table.

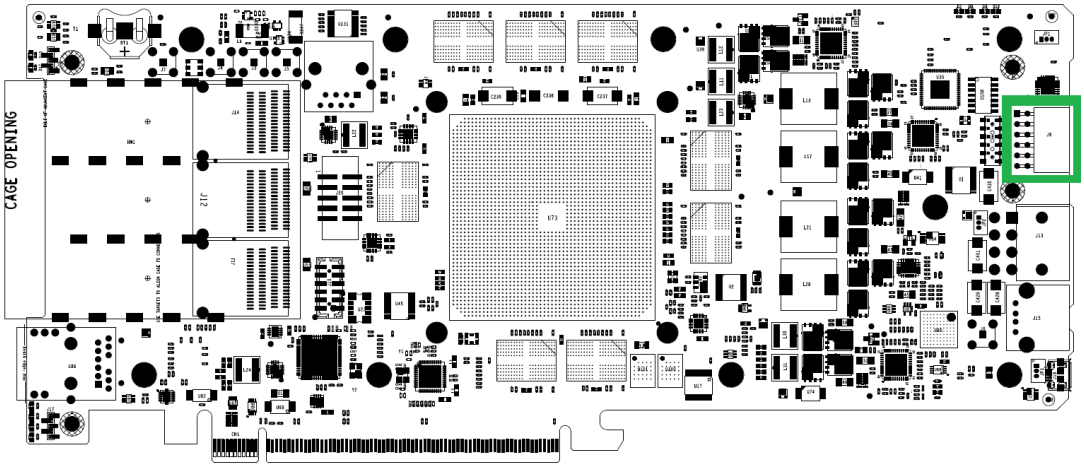


Figure 28 : PMOD location

3.15 Fan Speed Control

The ADM-PA120 uses a fan speed controller to drive and monitor the 3 built-in fans.

The fan controller is part number MAX6620ATI+

AVR2UTIL can be used to control fan speed. Reference the MAX6620 datasheet for register details.

Below are example avr2util raw i2c commands that can be used to change fan speeds using RPM mode.

Configure all fans for RPM mode:

```
avr2util.exe /usbcom \\.\com4 i2c-write 1 0x2a 0x00 0x00
avr2util.exe /usbcom \\.\com4 i2c-write 1 0x2a 0x01 0x00
avr2util.exe /usbcom \\.\com4 i2c-write 1 0x2a 0x02 0xC8
avr2util.exe /usbcom \\.\com4 i2c-write 1 0x2a 0x03 0xC8
avr2util.exe /usbcom \\.\com4 i2c-write 1 0x2a 0x04 0xC8
avr2util.exe /usbcom \\.\com4 i2c-write 1 0x2a 0x06 0x64
avr2util.exe /usbcom \\.\com4 i2c-write 1 0x2a 0x07 0x64
avr2util.exe /usbcom \\.\com4 i2c-write 1 0x2a 0x08 0x64
```

Set all fan speeds to 4K RPM:

```
avr2util.exe /usbcom \\.\com4 i2c-write 1 0x2a 0x20 0x40
avr2util.exe /usbcom \\.\com4 i2c-write 1 0x2a 0x21 0x00
avr2util.exe /usbcom \\.\com4 i2c-write 1 0x2a 0x22 0x40
avr2util.exe /usbcom \\.\com4 i2c-write 1 0x2a 0x23 0x00
avr2util.exe /usbcom \\.\com4 i2c-write 1 0x2a 0x24 0x40
avr2util.exe /usbcom \\.\com4 i2c-write 1 0x2a 0x25 0x00
```

Set all fan speeds to 10K RPM:

```
avr2util.exe /usbcom \\.\com4 i2c-write 1 0x2a 0x20 0x19
avr2util.exe /usbcom \\.\com4 i2c-write 1 0x2a 0x21 0x00
avr2util.exe /usbcom \\.\com4 i2c-write 1 0x2a 0x22 0x19
avr2util.exe /usbcom \\.\com4 i2c-write 1 0x2a 0x23 0x00
avr2util.exe /usbcom \\.\com4 i2c-write 1 0x2a 0x24 0x19
avr2util.exe /usbcom \\.\com4 i2c-write 1 0x2a 0x25 0x00
```

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Appendix A: MIO Map

Pin Number	Pin Name	Signal Name	Comment
J13	PMC_MIO0_500	QSPI0_CLK	Dual-Parallel Quad SPI
K13	PMC_MIO1_500	QSPI0_IO[1]	Dual-Parallel Quad SPI
L13	PMC_MIO2_500	QSPI0_IO[2]	Dual-Parallel Quad SPI
M13	PMC_MIO3_500	QSPI0_IO[3]	Dual-Parallel Quad SPI
P13	PMC_MIO4_500	QSPI0_IO[0]	Dual-Parallel Quad SPI
R13	PMC_MIO5_500	QSPI0_CS_b	Dual-Parallel Quad SPI
T13	PMC_MIO6_500	NC	-
U13	PMC_MIO7_500	QSPI1_CS_b	Dual-Parallel Quad SPI
V14	PMC_MIO8_500	QSPI1_IO[0]	Dual-Parallel Quad SPI
U14	PMC_MIO9_500	QSPI1_IO[1]	Dual-Parallel Quad SPI
T14	PMC_MIO10_500	QSPI1_IO[2]	Dual-Parallel Quad SPI
P14	PMC_MIO11_500	QSPI1_IO[3]	Dual-Parallel Quad SPI
N14	PMC_MIO12_500	QSPI1_CLK	Dual-Parallel Quad SPI
M14	PMC_MIO13_500	USB_ULPI_RST	USB 2.0
L14	PMC_MIO14_500	USB_ULPI_DATA[0]	USB 2.0
J14	PMC_MIO15_500	USB_ULPI_DATA[1]	USB 2.0
J15	PMC_MIO16_500	USB_ULPI_DATA[2]	USB 2.0
K15	PMC_MIO17_500	USB_ULPI_DATA[3]	USB 2.0
L15	PMC_MIO18_500	USB_ULPI_CLK	USB 2.0
N15	PMC_MIO19_500	USB_ULPI_DATA[4]	USB 2.0
P15	PMC_MIO20_500	USB_ULPI_DATA[5]	USB 2.0
R15	PMC_MIO21_500	USB_ULPI_DATA[6]	USB 2.0
T15	PMC_MIO22_500	USB_ULPI_DATA[7]	USB 2.0
V15	PMC_MIO23_500	USB_ULPI_DIR	USB 2.0
V16	PMC_MIO24_500	USB_ULPI_STP	USB 2.0
U16	PMC_MIO25_500	USB_ULPI_NXT	USB 2.0
T16	PMC_MIO26_501	SD1_CLK	SD1_3.0
R16	PMC_MIO27_501	NC	-
N16	PMC_MIO28_501	SD1_DETECT	SD1_3.0
M16	PMC_MIO29_501	SD1_CMD	SD1_3.0
L16	PMC_MIO30_501	SD1_DATA[0]	SD1_3.0
K16	PMC_MIO31_501	SD1_DATA[1]	SD1_3.0
M17	PMC_MIO32_501	SD1_DATA[2]	SD1_3.0
N17	PMC_MIO33_501	SD1_DATA[3]	SD1_3.0

Table 11 : MIO Map (continued on next page)

Pin Number	Pin Name	Signal Name	Comment
P17	PMC_MIO34_501	SD1_SEL	SD1_3.0
R17	PMC_MIO35_501	NC	-
U17	PMC_MIO36_501	NC	-
V17	PMC_MIO37_501	GEM0_RST_L	GEM0 Ethernet
W17	PMC_MIO38_501	PCIE_PERST_B	PCIE
W18	PMC_MIO39_501	PCIE_PERST_B	PCIE
U18	PMC_MIO40_501	NC	-
T18	PMC_MIO41_501	NC	-
R18	PMC_MIO42_501	UART0_RXD	Not availabe until full power
P18	PMC_MIO43_501	UART0_TXD	Not availabe until full power
M18	PMC_MIO44_501	NC	-
M19	PMC_MIO45_501	NC	-
N19	PMC_MIO46_501	UART1_RXD	Available with aux. power
P19	PMC_MIO47_501	UART1_TXD	Available with aux. power
T19	PMC_MIO48_501	LPD_I2C1_SCL	Not Used
U19	PMC_MIO49_501	LPD_I2C1_SDA	Not Used
V19	PMC_MIO50_501	PMC_I2C_SCL	Not Used
N20	PMC_MIO51_501	PMC_I2C_SDA	Not Used
G16	LPD_MIO0_502	GEM0_TX_CLK	GEM0 Ethernet
H16	LPD_MIO1_502	GEM0_TX_DATA[0]	GEM0 Ethernet
K17	LPD_MIO2_502	GEM0_TX_DATA[1]	GEM0 Ethernet
J17	LPD_MIO3_502	GEM0_TX_DATA[2]	GEM0 Ethernet
H17	LPD_MIO4_502	GEM0_TX_DATA[3]	GEM0 Ethernet
G17	LPD_MIO5_502	GEM0_TX_CTRL	GEM0 Ethernet
E17	LPD_MIO6_502	GEM0_RX_CLK	GEM0 Ethernet
D17	LPD_MIO7_502	GEM0_RX_DATA[0]	GEM0 Ethernet
D18	LPD_MIO8_502	GEM0_RX_DATA[1]	GEM0 Ethernet
E18	LPD_MIO9_502	GEM0_RX_DATA[2]	GEM0 Ethernet
F18	LPD_MIO10_502	GEM0_RX_DATA[3]	GEM0 Ethernet
G18	LPD_MIO11_502	GEM0_RX_CTRL	GEM0 Ethernet
J18	LPD_MIO12_502	NC	-
K18	LPD_MIO13_502	NC	-
L18	LPD_MIO14_502	NC	-
L19	LPD_MIO15_502	NC	-
J19	LPD_MIO16_502	NC	-
H19	LPD_MIO17_502	NC	-

Table 11 : MIO Map (continued on next page)

Pin Number	Pin Name	Signal Name	Comment
G19	LPD_MIO18_502	NC	-
F19	LPD_MIO19_502	NC	-
E20	LPD_MIO20_502	NC	-
F20	LPD_MIO21_502	NC	-
H20	LPD_MIO22_502	NC	-
J20	LPD_MIO23_502	NC	-
K20	LPD_MIO24_502	GEM0_MDIO_CLK	GEM0 Ethernet
L20	LPD_MIO25_502	GEM0_MDIO_DATA	GEM0 Ethernet

Table 11 : MIO Map

Appendix B: Complete Pinout Table

Note:
For customers using the /C1 version of this product, the LPDDR4 pinout is slightly different. Please contact support@alpha-data.com if you need additional details.

Pin Number	Signal Name	Pin Name	IO Voltage	Bank
R35	10MHZ_PIN_N	IO_L12N_GC_XCC_N4P1_712	1.5	712
T35	10MHZ_PIN_P	IO_L12P_GC_XCC_N4P0_712	1.5	712
P34	1PPS_FPGA	IO_L25P_N8P2_712	1.5	712
P35	485_0_DATA_FPGA	IO_L26P_N8P4_712	1.5	712
N37	485_0_DE/RE_L_FPGA	IO_L10P_N3P2_712	1.5	712
N35	485_1_DATA_FPGA	IO_L26N_N8P5_712	1.5	712
M33	485_1_DE/RE_L_FPGA	IO_L11P_N3P4_712	1.5	712
K36	AVR_B2U_1V5	IO_L0P_XCC_N0P0_712	1.5	712
L36	AVR_MON_CLK_1V5	IO_L1P_N0P2_712	1.5	712
K35	AVR_U2B_1V5	IO_L0N_XCC_N0P1_712	1.5	712
BF24	DO_NOT_USE	IO_L26N_N8P5_M1P107_704	1.1	704
BF23	DO_NOT_USE	IO_L26P_N8P4_M1P106_704	1.1	704
BD40	DO_NOT_USE	IO_L25N_N8P3_M2P105_707	1.1	707
BC40	DO_NOT_USE	IO_L26P_N8P4_M2P106_707	1.1	707
AL42	DO_NOT_USE	IO_L24N_GC_XCC_N8P1_M2P157_708	1.1	708
AK43	DO_NOT_USE	IO_L24P_GC_XCC_N8P0_M2P156_708	1.1	708
AM43	DO_NOT_USE	IO_L25P_N8P2_M2P158_708	1.1	708
AP44	DO_NOT_USE	IO_L26N_N8P5_M2P161_708	1.1	708
L24	DO_NOT_USE	IO_L24N_GC_XCC_N8P1_M3P49_709	1.1	709
M24	DO_NOT_USE	IO_L24P_GC_XCC_N8P0_M3P48_709	1.1	709
L23	DO_NOT_USE	IO_L25P_N8P2_M3P50_709	1.1	709
K21	DO_NOT_USE	IO_L26N_N8P5_M3P53_709	1.1	709
K25	DO_NOT_USE	IO_L24N_GC_XCC_N8P1_M3P103_710	1.1	710
K26	DO_NOT_USE	IO_L24P_GC_XCC_N8P0_M3P102_710	1.1	710
K27	DO_NOT_USE	IO_L25P_N8P2_M3P104_710	1.1	710
H25	DO_NOT_USE	IO_L26N_N8P5_M3P107_710	1.1	710
M34	FABRIC_CLK_1V5 (refclk_100m)	IO_L9P_GC_XCC_N3P0_712	1.5	712
BD39	FAN_FAIL_1V1_L	IO_L25P_N8P2_M2P104_707	1.1	707
K20	GEM0_MDC	LPD_MIO24_502	3.3	502
L20	GEM0_MDIO	LPD_MIO25_502	3.3	502

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage	Bank
V17	GEM0_RST_L	PMC_MIO37_501	1.8	501
E17	GEM0_RX_CLK	LPD_MIO6_502	3.3	502
G18	GEM0_RX_CTRL	LPD_MIO11_502	3.3	502
D17	GEM0_RXD_0	LPD_MIO7_502	3.3	502
D18	GEM0_RXD_1	LPD_MIO8_502	3.3	502
E18	GEM0_RXD_2	LPD_MIO9_502	3.3	502
F18	GEM0_RXD_3	LPD_MIO10_502	3.3	502
G16	GEM0_TX_CLK	LPD_MIO0_502	3.3	502
G17	GEM0_TX_CTRL	LPD_MIO5_502	3.3	502
H16	GEM0_TXD_0	LPD_MIO1_502	3.3	502
K17	GEM0_TXD_1	LPD_MIO2_502	3.3	502
J17	GEM0_TXD_2	LPD_MIO3_502	3.3	502
H17	GEM0_TXD_3	LPD_MIO4_502	3.3	502
AM13	LPDDR4_0_CH0_CA_A[0]	IO_L22N_N7P3_M0P45_700	1.1	700
AL14	LPDDR4_0_CH0_CA_A[1]	IO_L22P_N7P2_M0P44_700	1.1	700
AK13	LPDDR4_0_CH0_CA_A[2]	IO_L21P_XCC_N7P0_M0P42_700	1.1	700
AN13	LPDDR4_0_CH0_CA_A[3]	IO_L23N_N7P5_M0P47_700	1.1	700
AJ12	LPDDR4_0_CH0_CA_A[4]	IO_L19P_N6P2_M0P38_700	1.1	700
AJ13	LPDDR4_0_CH0_CA_A[5]	IO_L19N_N6P3_M0P39_700	1.1	700
AT13	LPDDR4_0_CH0_CA_B[0]	IO_L16P_N5P2_M0P32_700	1.1	700
AR13	LPDDR4_0_CH0_CA_B[1]	IO_L14N_N4P5_M0P29_700	1.1	700
AV13	LPDDR4_0_CH0_CA_B[2]	IO_L17N_N5P5_M0P35_700	1.1	700
AU14	LPDDR4_0_CH0_CA_B[3]	IO_L17P_N5P4_M0P34_700	1.1	700
AR12	LPDDR4_0_CH0_CA_B[4]	IO_L13N_N4P3_M0P27_700	1.1	700
AP11	LPDDR4_0_CH0_CA_B[5]	IO_L13P_N4P2_M0P26_700	1.1	700
AK14	LPDDR4_0_CH0_CK_C_A[0]	IO_L18N_XCC_N6P1_M0P37_700	1.1	700
AP15	LPDDR4_0_CH0_CK_C_B[0]	IO_L12N_GC_XCC_N4P1_M0P25_700	1.1	700
AJ15	LPDDR4_0_CH0_CK_T_A[0]	IO_L18P_XCC_N6P0_M0P36_700	1.1	700
AN14	LPDDR4_0_CH0_CK_T_B[0]	IO_L12P_GC_XCC_N4P0_M0P24_700	1.1	700
AL15	LPDDR4_0_CH0_CKE_A[0]	IO_L20P_N6P4_M0P40_700	1.1	700
AM15	LPDDR4_0_CH0_CKE_A[1]	IO_L20N_N6P5_M0P41_700	1.1	700
AP12	LPDDR4_0_CH0_CKE_B[0]	IO_L14P_N4P4_M0P28_700	1.1	700
AT14	LPDDR4_0_CH0_CKE_B[1]	IO_L16N_N5P3_M0P33_700	1.1	700
AM12	LPDDR4_0_CH0_CS_A[0]	IO_L23P_N7P4_M0P46_700	1.1	700
AL12	LPDDR4_0_CH0_CS_A[1]	IO_L21N_XCC_N7P1_M0P43_700	1.1	700
BD12	LPDDR4_0_CH0_CS_B[0]	IO_L0N_XCC_N0P1_M0P1_700	1.1	700

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage	Bank
BA9	LPDDR4_0_CH0_CS_B[1]	IO_L9N_GC_XCC_N3P1_M0P19_700	1.1	700
AY9	LPDDR4_0_CH0_DMI_A[0]	IO_L0P_XCC_N0P0_M0P0_700	1.1	700
BG9	LPDDR4_0_CH0_DMI_A[1]	IO_L3P_XCC_N1P0_M0P60_701	1.1	701
BC13	LPDDR4_0_CH0_DMI_B[0]	IO_L9P_GC_XCC_N3P0_M0P18_700	1.1	700
BH4	LPDDR4_0_CH0_DMI_B[1]	IO_L15P_XCC_N5P0_M0P84_701	1.1	701
AY12	LPDDR4_0_CH0_DQ_A[0]	IO_L2N_N0P5_M0P5_700	1.1	700
AW13	LPDDR4_0_CH0_DQ_A[1]	IO_L2P_N0P4_M0P4_700	1.1	700
BH10	LPDDR4_0_CH0_DQ_A[10]	IO_L5N_N1P5_M0P65_701	1.1	701
BG12	LPDDR4_0_CH0_DQ_A[11]	IO_L4P_N1P2_M0P62_701	1.1	701
BH12	LPDDR4_0_CH0_DQ_A[12]	IO_L2N_N0P5_M0P59_701	1.1	701
BG13	LPDDR4_0_CH0_DQ_A[13]	IO_L2P_N0P4_M0P58_701	1.1	701
BF11	LPDDR4_0_CH0_DQ_A[14]	IO_L1N_N0P3_M0P57_701	1.1	701
BE12	LPDDR4_0_CH0_DQ_A[15]	IO_L1P_N0P2_M0P56_701	1.1	701
AY11	LPDDR4_0_CH0_DQ_A[2]	IO_L1N_N0P3_M0P3_700	1.1	700
AW11	LPDDR4_0_CH0_DQ_A[3]	IO_L1P_N0P2_M0P2_700	1.1	700
BB11	LPDDR4_0_CH0_DQ_A[4]	IO_L5N_N1P5_M0P11_700	1.1	700
BA12	LPDDR4_0_CH0_DQ_A[5]	IO_L5P_N1P4_M0P10_700	1.1	700
BB12	LPDDR4_0_CH0_DQ_A[6]	IO_L4N_N1P3_M0P9_700	1.1	700
BA13	LPDDR4_0_CH0_DQ_A[7]	IO_L4P_N1P2_M0P8_700	1.1	700
BG10	LPDDR4_0_CH0_DQ_A[8]	IO_L5P_N1P4_M0P64_701	1.1	701
BH11	LPDDR4_0_CH0_DQ_A[9]	IO_L4N_N1P3_M0P63_701	1.1	701
BD10	LPDDR4_0_CH0_DQ_B[0]	IO_L10P_N3P2_M0P20_700	1.1	700
BC12	LPDDR4_0_CH0_DQ_B[1]	IO_L8P_N2P4_M0P16_700	1.1	700
BJ2	LPDDR4_0_CH0_DQ_B[10]	IO_L17P_N5P4_M0P88_701	1.1	701
BL3	LPDDR4_0_CH0_DQ_B[11]	IO_L14N_N4P5_M0P83_701	1.1	701
BK5	LPDDR4_0_CH0_DQ_B[12]	IO_L13N_N4P3_M0P81_701	1.1	701
BJ5	LPDDR4_0_CH0_DQ_B[13]	IO_L13P_N4P2_M0P80_701	1.1	701
BJ3	LPDDR4_0_CH0_DQ_B[14]	IO_L16P_N5P2_M0P86_701	1.1	701
BL4	LPDDR4_0_CH0_DQ_B[15]	IO_L14P_N4P4_M0P82_701	1.1	701
BE9	LPDDR4_0_CH0_DQ_B[2]	IO_L11P_N3P4_M0P22_700	1.1	700
BD11	LPDDR4_0_CH0_DQ_B[3]	IO_L8N_N2P5_M0P17_700	1.1	700
BA10	LPDDR4_0_CH0_DQ_B[4]	IO_L7P_N2P2_M0P14_700	1.1	700
BB10	LPDDR4_0_CH0_DQ_B[5]	IO_L7N_N2P3_M0P15_700	1.1	700
BE10	LPDDR4_0_CH0_DQ_B[6]	IO_L10N_N3P3_M0P21_700	1.1	700
BF10	LPDDR4_0_CH0_DQ_B[7]	IO_L11N_N3P5_M0P23_700	1.1	700
BK2	LPDDR4_0_CH0_DQ_B[8]	IO_L17N_N5P5_M0P89_701	1.1	701

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage	Bank
BK3	LPDDR4_0_CH0_DQ_B[9]	IO_L16N_N5P3_M0P87_701	1.1	701
AY14	LPDDR4_0_CH0_DQS_C_A[0]	IO_L3N_XCC_N1P1_M0P7_700	1.1	700
BF12	LPDDR4_0_CH0_DQS_C_A[1]	IO_L0N_XCC_N0P1_M0P55_701	1.1	701
BC10	LPDDR4_0_CH0_DQS_C_B[0]	IO_L6N_GC_XCC_N2P1_M0P13_700	1.1	700
BK6	LPDDR4_0_CH0_DQS_C_B[1]	IO_L12N_GC_XCC_N4P1_M0P79_701	1.1	701
AW14	LPDDR4_0_CH0_DQS_T_A[0]	IO_L3P_XCC_N1P0_M0P6_700	1.1	700
BE13	LPDDR4_0_CH0_DQS_T_A[1]	IO_L0P_XCC_N0P0_M0P54_701	1.1	701
BC9	LPDDR4_0_CH0_DQS_T_B[0]	IO_L6P_GC_XCC_N2P0_M0P12_700	1.1	700
BJ7	LPDDR4_0_CH0_DQS_T_B[1]	IO_L12P_GC_XCC_N4P0_M0P78_701	1.1	701
AT10	LPDDR4_0_CH0_RESET_N[0]	IO_L25P_N8P2_M0P50_700	1.1	700
BN16	LPDDR4_0_CH1_CA_A[0]	IO_L4N_N1P3_M0P117_702	1.1	702
BM17	LPDDR4_0_CH1_CA_A[1]	IO_L4P_N1P2_M0P116_702	1.1	702
BN15	LPDDR4_0_CH1_CA_A[2]	IO_L5N_N1P5_M0P119_702	1.1	702
BM16	LPDDR4_0_CH1_CA_A[3]	IO_L5P_N1P4_M0P118_702	1.1	702
BK16	LPDDR4_0_CH1_CA_A[4]	IO_L1P_N0P2_M0P110_702	1.1	702
BL15	LPDDR4_0_CH1_CA_A[5]	IO_L1N_N0P3_M0P111_702	1.1	702
BC16	LPDDR4_0_CH1_CA_B[0]	IO_L14P_N4P4_M0P136_702	1.1	702
BD16	LPDDR4_0_CH1_CA_B[1]	IO_L14N_N4P5_M0P137_702	1.1	702
BF16	LPDDR4_0_CH1_CA_B[2]	IO_L17N_N5P5_M0P143_702	1.1	702
BB15	LPDDR4_0_CH1_CA_B[3]	IO_L13N_N4P3_M0P135_702	1.1	702
BB14	LPDDR4_0_CH1_CA_B[4]	IO_L13P_N4P2_M0P134_702	1.1	702
BE17	LPDDR4_0_CH1_CA_B[5]	IO_L17P_N5P4_M0P142_702	1.1	702
BL16	LPDDR4_0_CH1_CK_C_A[0]	IO_L0N_XCC_N0P1_M0P109_702	1.1	702
BC17	LPDDR4_0_CH1_CK_C_B[0]	IO_L12N_GC_XCC_N4P1_M0P133_702	1.1	702
BK17	LPDDR4_0_CH1_CK_T_A[0]	IO_L0P_XCC_N0P0_M0P108_702	1.1	702
BB16	LPDDR4_0_CH1_CK_T_B[0]	IO_L12P_GC_XCC_N4P0_M0P132_702	1.1	702
BM18	LPDDR4_0_CH1_CKE_A[0]	IO_L2P_N0P4_M0P112_702	1.1	702
BN14	LPDDR4_0_CH1_CKE_A[1]	IO_L3N_XCC_N1P1_M0P115_702	1.1	702
BE16	LPDDR4_0_CH1_CKE_B[0]	IO_L15N_XCC_N5P1_M0P139_702	1.1	702
BD15	LPDDR4_0_CH1_CKE_B[1]	IO_L15P_XCC_N5P0_M0P138_702	1.1	702
BM14	LPDDR4_0_CH1_CS_A[0]	IO_L3P_XCC_N1P0_M0P114_702	1.1	702
BN17	LPDDR4_0_CH1_CS_A[1]	IO_L2N_N0P5_M0P113_702	1.1	702
BJ18	LPDDR4_0_CH1_CS_B[0]	IO_L6N_GC_XCC_N2P1_M0P121_702	1.1	702
AW16	LPDDR4_0_CH1_CS_B[1]	IO_L21N_XCC_N7P1_M0P151_702	1.1	702
BH17	LPDDR4_0_CH1_DMI_A[0]	IO_L6P_GC_XCC_N2P0_M0P120_702	1.1	702
BL13	LPDDR4_0_CH1_DMI_A[1]	IO_L18P_XCC_N6P0_M0P90_701	1.1	701

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage	Bank
AV15	LPDDR4_0_CH1_DMI_B[0]	IO_L21P_XCC_N7P0_M0P150_702	1.1	702
BM6	LPDDR4_0_CH1_DMI_B[1]	IO_L9P_GC_XCC_N3P0_M0P72_701	1.1	701
BK15	LPDDR4_0_CH1_DQ_A[0]	IO_L11P_N3P4_M0P130_702	1.1	702
BL14	LPDDR4_0_CH1_DQ_A[1]	IO_L11N_N3P5_M0P131_702	1.1	702
BJ12	LPDDR4_0_CH1_DQ_A[10]	IO_L19P_N6P2_M0P92_701	1.1	701
BN12	LPDDR4_0_CH1_DQ_A[11]	IO_L20N_N6P5_M0P95_701	1.1	701
BK10	LPDDR4_0_CH1_DQ_A[12]	IO_L23N_N7P5_M0P101_701	1.1	701
BL10	LPDDR4_0_CH1_DQ_A[13]	IO_L22N_N7P3_M0P99_701	1.1	701
BK11	LPDDR4_0_CH1_DQ_A[14]	IO_L19N_N6P3_M0P93_701	1.1	701
BL11	LPDDR4_0_CH1_DQ_A[15]	IO_L22P_N7P2_M0P98_701	1.1	701
BJ14	LPDDR4_0_CH1_DQ_A[2]	IO_L7N_N2P3_M0P123_702	1.1	702
BH14	LPDDR4_0_CH1_DQ_A[3]	IO_L7P_N2P2_M0P122_702	1.1	702
BL18	LPDDR4_0_CH1_DQ_A[4]	IO_L10N_N3P3_M0P129_702	1.1	702
BK18	LPDDR4_0_CH1_DQ_A[5]	IO_L10P_N3P2_M0P128_702	1.1	702
BJ17	LPDDR4_0_CH1_DQ_A[6]	IO_L8N_N2P5_M0P125_702	1.1	702
BH16	LPDDR4_0_CH1_DQ_A[7]	IO_L8P_N2P4_M0P124_702	1.1	702
BM12	LPDDR4_0_CH1_DQ_A[8]	IO_L20P_N6P4_M0P94_701	1.1	701
BJ10	LPDDR4_0_CH1_DQ_A[9]	IO_L23P_N7P4_M0P100_701	1.1	701
AV16	LPDDR4_0_CH1_DQ_B[0]	IO_L20P_N6P4_M0P148_702	1.1	702
AW17	LPDDR4_0_CH1_DQ_B[1]	IO_L20N_N6P5_M0P149_702	1.1	702
BN5	LPDDR4_0_CH1_DQ_B[10]	IO_L10P_N3P2_M0P74_701	1.1	701
BM4	LPDDR4_0_CH1_DQ_B[11]	IO_L10N_N3P3_M0P75_701	1.1	701
BL5	LPDDR4_0_CH1_DQ_B[12]	IO_L11N_N3P5_M0P77_701	1.1	701
BL6	LPDDR4_0_CH1_DQ_B[13]	IO_L11P_N3P4_M0P76_701	1.1	701
BK7	LPDDR4_0_CH1_DQ_B[14]	IO_L7N_N2P3_M0P69_701	1.1	701
BL8	LPDDR4_0_CH1_DQ_B[15]	IO_L7P_N2P2_M0P68_701	1.1	701
AY17	LPDDR4_0_CH1_DQ_B[2]	IO_L22P_N7P2_M0P152_702	1.1	702
AY15	LPDDR4_0_CH1_DQ_B[3]	IO_L23P_N7P4_M0P154_702	1.1	702
BA16	LPDDR4_0_CH1_DQ_B[4]	IO_L22N_N7P3_M0P153_702	1.1	702
BA15	LPDDR4_0_CH1_DQ_B[5]	IO_L23N_N7P5_M0P155_702	1.1	702
AT16	LPDDR4_0_CH1_DQ_B[6]	IO_L19P_N6P2_M0P146_702	1.1	702
AU15	LPDDR4_0_CH1_DQ_B[7]	IO_L19N_N6P3_M0P147_702	1.1	702
BN7	LPDDR4_0_CH1_DQ_B[8]	IO_L8N_N2P5_M0P71_701	1.1	701
BM7	LPDDR4_0_CH1_DQ_B[9]	IO_L8P_N2P4_M0P70_701	1.1	701
BJ15	LPDDR4_0_CH1_DQS_C_A[0]	IO_L9N_GC_XCC_N3P1_M0P127_702	1.1	702
BN11	LPDDR4_0_CH1_DQS_C_A[1]	IO_L21N_XCC_N7P1_M0P97_701	1.1	701

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage	Bank
AU17	LPDDR4_0_CH1_DQS_C_B[0]	IO_L18N_XCC_N6P1_M0P145_702	1.1	702
BM8	LPDDR4_0_CH1_DQS_C_B[1]	IO_L6N_GC_XCC_N2P1_M0P67_701	1.1	701
BH15	LPDDR4_0_CH1_DQS_T_A[0]	IO_L9P_GC_XCC_N3P0_M0P126_702	1.1	702
BM11	LPDDR4_0_CH1_DQS_T_A[1]	IO_L21P_XCC_N7P0_M0P96_701	1.1	701
AT17	LPDDR4_0_CH1_DQS_T_B[0]	IO_L18P_XCC_N6P0_M0P144_702	1.1	702
BN9	LPDDR4_0_CH1_DQS_T_B[1]	IO_L6P_GC_XCC_N2P0_M0P66_701	1.1	701
AU9	LPDDR4_0_CH1_RESET_N[0]	IO_L25N_N8P3_M0P51_700	1.1	700
AW22	LPDDR4_1_CH0_CA_A[0]	IO_L22N_N7P3_M1P45_703	1.1	703
AV22	LPDDR4_1_CH0_CA_A[1]	IO_L22P_N7P2_M1P44_703	1.1	703
AV18	LPDDR4_1_CH0_CA_A[2]	IO_L21P_XCC_N7P0_M1P42_703	1.1	703
AW20	LPDDR4_1_CH0_CA_A[3]	IO_L23N_N7P5_M1P47_703	1.1	703
AT19	LPDDR4_1_CH0_CA_A[4]	IO_L19P_N6P2_M1P38_703	1.1	703
AU18	LPDDR4_1_CH0_CA_A[5]	IO_L19N_N6P3_M1P39_703	1.1	703
BB22	LPDDR4_1_CH0_CA_B[0]	IO_L16P_N5P2_M1P32_703	1.1	703
BA21	LPDDR4_1_CH0_CA_B[1]	IO_L14N_N4P5_M1P29_703	1.1	703
BB20	LPDDR4_1_CH0_CA_B[2]	IO_L17N_N5P5_M1P35_703	1.1	703
BB19	LPDDR4_1_CH0_CA_B[3]	IO_L17P_N5P4_M1P34_703	1.1	703
BA18	LPDDR4_1_CH0_CA_B[4]	IO_L13N_N4P3_M1P27_703	1.1	703
AY18	LPDDR4_1_CH0_CA_B[5]	IO_L13P_N4P2_M1P26_703	1.1	703
AU21	LPDDR4_1_CH0_CK_C_A[0]	IO_L18N_XCC_N6P1_M1P37_703	1.1	703
BA22	LPDDR4_1_CH0_CK_C_B[0]	IO_L12N_GC_XCC_N4P1_M1P25_703	1.1	703
AT20	LPDDR4_1_CH0_CK_T_A[0]	IO_L18P_XCC_N6P0_M1P36_703	1.1	703
AY21	LPDDR4_1_CH0_CK_T_B[0]	IO_L12P_GC_XCC_N4P0_M1P24_703	1.1	703
AU20	LPDDR4_1_CH0_CKE_A[0]	IO_L20P_N6P4_M1P40_703	1.1	703
AV21	LPDDR4_1_CH0_CKE_A[1]	IO_L20N_N6P5_M1P41_703	1.1	703
AY20	LPDDR4_1_CH0_CKE_B[0]	IO_L14P_N4P4_M1P28_703	1.1	703
BC21	LPDDR4_1_CH0_CKE_B[1]	IO_L16N_N5P3_M1P33_703	1.1	703
AV19	LPDDR4_1_CH0_CS_A[0]	IO_L23P_N7P4_M1P46_703	1.1	703
AW19	LPDDR4_1_CH0_CS_A[1]	IO_L21N_XCC_N7P1_M1P43_703	1.1	703
BL21	LPDDR4_1_CH0_CS_B[0]	IO_L0N_XCC_N0P1_M1P1_703	1.1	703
BJ19	LPDDR4_1_CH0_CS_B[1]	IO_L9N_GC_XCC_N3P1_M1P19_703	1.1	703
AW23	LPDDR4_1_CH0_DMI_A[0]	IO_L15P_XCC_N5P0_M1P84_704	1.1	704
BH20	LPDDR4_1_CH0_DMI_A[1]	IO_L9P_GC_XCC_N3P0_M1P18_703	1.1	703
BL23	LPDDR4_1_CH0_DMI_B[0]	IO_L3P_XCC_N1P0_M1P60_704	1.1	704
BK22	LPDDR4_1_CH0_DMI_B[1]	IO_L0P_XCC_N0P0_M1P0_703	1.1	703
BB24	LPDDR4_1_CH0_DQ_A[0]	IO_L17P_N5P4_M1P88_704	1.1	704

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage	Bank
BC24	LPDDR4_1_CH0_DQ_A[1]	IO_L17N_N5P5_M1P89_704	1.1	704
BJ22	LPDDR4_1_CH0_DQ_A[10]	IO_L10N_N3P3_M1P21_703	1.1	703
BK20	LPDDR4_1_CH0_DQ_A[11]	IO_L11N_N3P5_M1P23_703	1.1	703
BH22	LPDDR4_1_CH0_DQ_A[12]	IO_L8N_N2P5_M1P17_703	1.1	703
BG21	LPDDR4_1_CH0_DQ_A[13]	IO_L8P_N2P4_M1P16_703	1.1	703
BH21	LPDDR4_1_CH0_DQ_A[14]	IO_L10P_N3P2_M1P20_703	1.1	703
BG20	LPDDR4_1_CH0_DQ_A[15]	IO_L7P_N2P2_M1P14_703	1.1	703
BB23	LPDDR4_1_CH0_DQ_A[2]	IO_L16N_N5P3_M1P87_704	1.1	704
BA24	LPDDR4_1_CH0_DQ_A[3]	IO_L16P_N5P2_M1P86_704	1.1	704
AT25	LPDDR4_1_CH0_DQ_A[4]	IO_L14P_N4P4_M1P82_704	1.1	704
AV24	LPDDR4_1_CH0_DQ_A[5]	IO_L13N_N4P3_M1P81_704	1.1	704
AU24	LPDDR4_1_CH0_DQ_A[6]	IO_L14N_N4P5_M1P83_704	1.1	704
AU23	LPDDR4_1_CH0_DQ_A[7]	IO_L13P_N4P2_M1P80_704	1.1	704
BH19	LPDDR4_1_CH0_DQ_A[8]	IO_L7N_N2P3_M1P15_703	1.1	703
BJ20	LPDDR4_1_CH0_DQ_A[9]	IO_L11P_N3P4_M1P22_703	1.1	703
BL24	LPDDR4_1_CH0_DQ_B[0]	IO_L4P_N1P2_M1P62_704	1.1	704
BN24	LPDDR4_1_CH0_DQ_B[1]	IO_L5P_N1P4_M1P64_704	1.1	704
BN21	LPDDR4_1_CH0_DQ_B[10]	IO_L5N_N1P5_M1P11_703	1.1	703
BM21	LPDDR4_1_CH0_DQ_B[11]	IO_L5P_N1P4_M1P10_703	1.1	703
BM19	LPDDR4_1_CH0_DQ_B[12]	IO_L2N_N0P5_M1P5_703	1.1	703
BK21	LPDDR4_1_CH0_DQ_B[13]	IO_L1P_N0P2_M1P2_703	1.1	703
BL20	LPDDR4_1_CH0_DQ_B[14]	IO_L1N_N0P3_M1P3_703	1.1	703
BL19	LPDDR4_1_CH0_DQ_B[15]	IO_L2P_N0P4_M1P4_703	1.1	703
BM24	LPDDR4_1_CH0_DQ_B[2]	IO_L4N_N1P3_M1P63_704	1.1	704
BN25	LPDDR4_1_CH0_DQ_B[3]	IO_L5N_N1P5_M1P65_704	1.1	704
BJ23	LPDDR4_1_CH0_DQ_B[4]	IO_L1P_N0P2_M1P56_704	1.1	704
BJ24	LPDDR4_1_CH0_DQ_B[5]	IO_L2P_N0P4_M1P58_704	1.1	704
BK25	LPDDR4_1_CH0_DQ_B[6]	IO_L2N_N0P5_M1P59_704	1.1	704
BK23	LPDDR4_1_CH0_DQ_B[7]	IO_L1N_N0P3_M1P57_704	1.1	704
BN22	LPDDR4_1_CH0_DQ_B[8]	IO_L4N_N1P3_M1P9_703	1.1	703
BM22	LPDDR4_1_CH0_DQ_B[9]	IO_L4P_N1P2_M1P8_703	1.1	703
AT23	LPDDR4_1_CH0_DQS_C_A[0]	IO_L12N_GC_XCC_N4P1_M1P79_704	1.1	704
BG22	LPDDR4_1_CH0_DQS_C_A[1]	IO_L6N_GC_XCC_N2P1_M1P13_703	1.1	703
BH24	LPDDR4_1_CH0_DQS_C_B[0]	IO_L0N_XCC_N0P1_M1P55_704	1.1	704
BN20	LPDDR4_1_CH0_DQS_C_B[1]	IO_L3N_XCC_N1P1_M1P7_703	1.1	703
AT22	LPDDR4_1_CH0_DQS_T_A[0]	IO_L12P_GC_XCC_N4P0_M1P78_704	1.1	704

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage	Bank
BF22	LPDDR4_1_CH0_DQS_T_A[1]	IO_L6P_GC_XCC_N2P0_M1P12_703	1.1	703
BG24	LPDDR4_1_CH0_DQS_T_B[0]	IO_L0P_XCC_N0P0_M1P54_704	1.1	704
BN19	LPDDR4_1_CH0_DQS_T_B[1]	IO_L3P_XCC_N1P0_M1P6_703	1.1	703
BE20	LPDDR4_1_CH0_RESET_N[0]	IO_L25P_N8P2_M1P50_703	1.1	703
BN31	LPDDR4_1_CH1_CA_A[0]	IO_L4N_N1P3_M1P117_705	1.1	705
BM31	LPDDR4_1_CH1_CA_A[1]	IO_L4P_N1P2_M1P116_705	1.1	705
BN30	LPDDR4_1_CH1_CA_A[2]	IO_L5N_N1P5_M1P119_705	1.1	705
BN29	LPDDR4_1_CH1_CA_A[3]	IO_L5P_N1P4_M1P118_705	1.1	705
BL28	LPDDR4_1_CH1_CA_A[4]	IO_L1P_N0P2_M1P110_705	1.1	705
BM28	LPDDR4_1_CH1_CA_A[5]	IO_L1N_N0P3_M1P111_705	1.1	705
BB30	LPDDR4_1_CH1_CA_B[0]	IO_L14P_N4P4_M1P136_705	1.1	705
BC30	LPDDR4_1_CH1_CA_B[1]	IO_L14N_N4P5_M1P137_705	1.1	705
BE28	LPDDR4_1_CH1_CA_B[2]	IO_L17N_N5P5_M1P143_705	1.1	705
BA28	LPDDR4_1_CH1_CA_B[3]	IO_L13N_N4P3_M1P135_705	1.1	705
AY29	LPDDR4_1_CH1_CA_B[4]	IO_L13P_N4P2_M1P134_705	1.1	705
BD28	LPDDR4_1_CH1_CA_B[5]	IO_L17P_N5P4_M1P142_705	1.1	705
BL31	LPDDR4_1_CH1_CK_C_A[0]	IO_L0N_XCC_N0P1_M1P109_705	1.1	705
BA30	LPDDR4_1_CH1_CK_C_B[0]	IO_L12N_GC_XCC_N4P1_M1P133_705	1.1	705
BK31	LPDDR4_1_CH1_CK_T_A[0]	IO_L0P_XCC_N0P0_M1P108_705	1.1	705
AY30	LPDDR4_1_CH1_CK_T_B[0]	IO_L12P_GC_XCC_N4P0_M1P132_705	1.1	705
BK30	LPDDR4_1_CH1_CKE_A[0]	IO_L2P_N0P4_M1P112_705	1.1	705
BM29	LPDDR4_1_CH1_CKE_A[1]	IO_L3N_XCC_N1P1_M1P115_705	1.1	705
BC28	LPDDR4_1_CH1_CKE_B[0]	IO_L15N_XCC_N5P1_M1P139_705	1.1	705
BB27	LPDDR4_1_CH1_CKE_B[1]	IO_L15P_XCC_N5P0_M1P138_705	1.1	705
BL30	LPDDR4_1_CH1_CS_A[0]	IO_L3P_XCC_N1P0_M1P114_705	1.1	705
BL29	LPDDR4_1_CH1_CS_A[1]	IO_L2N_N0P5_M1P113_705	1.1	705
BH31	LPDDR4_1_CH1_CS_B[0]	IO_L6N_GC_XCC_N2P1_M1P121_705	1.1	705
AW28	LPDDR4_1_CH1_CS_B[1]	IO_L21N_XCC_N7P1_M1P151_705	1.1	705
BG30	LPDDR4_1_CH1_DMI_A[0]	IO_L6P_GC_XCC_N2P0_M1P120_705	1.1	705
AT26	LPDDR4_1_CH1_DMI_A[1]	IO_L18P_XCC_N6P0_M1P90_704	1.1	704
AV27	LPDDR4_1_CH1_DMI_B[0]	IO_L21P_XCC_N7P0_M1P150_705	1.1	705
BK26	LPDDR4_1_CH1_DMI_B[1]	IO_L9P_GC_XCC_N3P0_M1P72_704	1.1	704
BJ28	LPDDR4_1_CH1_DQ_A[0]	IO_L11P_N3P4_M1P130_705	1.1	705
BH30	LPDDR4_1_CH1_DQ_A[1]	IO_L8P_N2P4_M1P124_705	1.1	705
BC25	LPDDR4_1_CH1_DQ_A[10]	IO_L22N_N7P3_M1P99_704	1.1	704
BB26	LPDDR4_1_CH1_DQ_A[11]	IO_L22P_N7P2_M1P98_704	1.1	704

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage	Bank
AY26	LPDDR4_1_CH1_DQ_A[12]	IO_L20P_N6P4_M1P94_704	1.1	704
BA25	LPDDR4_1_CH1_DQ_A[13]	IO_L20N_N6P5_M1P95_704	1.1	704
AW26	LPDDR4_1_CH1_DQ_A[14]	IO_L19N_N6P3_M1P93_704	1.1	704
AV25	LPDDR4_1_CH1_DQ_A[15]	IO_L19P_N6P2_M1P92_704	1.1	704
BH29	LPDDR4_1_CH1_DQ_A[2]	IO_L10P_N3P2_M1P128_705	1.1	705
BJ30	LPDDR4_1_CH1_DQ_A[3]	IO_L8N_N2P5_M1P125_705	1.1	705
BJ29	LPDDR4_1_CH1_DQ_A[4]	IO_L10N_N3P3_M1P129_705	1.1	705
BK28	LPDDR4_1_CH1_DQ_A[5]	IO_L11N_N3P5_M1P131_705	1.1	705
BG28	LPDDR4_1_CH1_DQ_A[6]	IO_L7N_N2P3_M1P123_705	1.1	705
BF27	LPDDR4_1_CH1_DQ_A[7]	IO_L7P_N2P2_M1P122_705	1.1	705
BD24	LPDDR4_1_CH1_DQ_A[8]	IO_L23P_N7P4_M1P100_704	1.1	704
BE25	LPDDR4_1_CH1_DQ_A[9]	IO_L23N_N7P5_M1P101_704	1.1	704
AT28	LPDDR4_1_CH1_DQ_B[0]	IO_L19P_N6P2_M1P146_705	1.1	705
AU27	LPDDR4_1_CH1_DQ_B[1]	IO_L19N_N6P3_M1P147_705	1.1	705
BN27	LPDDR4_1_CH1_DQ_B[10]	IO_L10N_N3P3_M1P75_704	1.1	704
BN26	LPDDR4_1_CH1_DQ_B[11]	IO_L11N_N3P5_M1P77_704	1.1	704
BJ25	LPDDR4_1_CH1_DQ_B[12]	IO_L7N_N2P3_M1P69_704	1.1	704
BH25	LPDDR4_1_CH1_DQ_B[13]	IO_L7P_N2P2_M1P68_704	1.1	704
BM26	LPDDR4_1_CH1_DQ_B[14]	IO_L11P_N3P4_M1P76_704	1.1	704
BK27	LPDDR4_1_CH1_DQ_B[15]	IO_L8P_N2P4_M1P70_704	1.1	704
AV28	LPDDR4_1_CH1_DQ_B[2]	IO_L20N_N6P5_M1P149_705	1.1	705
AY27	LPDDR4_1_CH1_DQ_B[3]	IO_L23P_N7P4_M1P154_705	1.1	705
BA27	LPDDR4_1_CH1_DQ_B[4]	IO_L23N_N7P5_M1P155_705	1.1	705
AW29	LPDDR4_1_CH1_DQ_B[5]	IO_L22N_N7P3_M1P153_705	1.1	705
AU29	LPDDR4_1_CH1_DQ_B[6]	IO_L20P_N6P4_M1P148_705	1.1	705
AV30	LPDDR4_1_CH1_DQ_B[7]	IO_L22P_N7P2_M1P152_705	1.1	705
BL26	LPDDR4_1_CH1_DQ_B[8]	IO_L8N_N2P5_M1P71_704	1.1	704
BM27	LPDDR4_1_CH1_DQ_B[9]	IO_L10P_N3P2_M1P74_704	1.1	704
BJ27	LPDDR4_1_CH1_DQS_C_A[0]	IO_L9N_GC_XCC_N3P1_M1P127_705	1.1	705
AW25	LPDDR4_1_CH1_DQS_C_A[1]	IO_L21N_XCC_N7P1_M1P97_704	1.1	704
AU30	LPDDR4_1_CH1_DQS_C_B[0]	IO_L18N_XCC_N6P1_M1P145_705	1.1	705
BH26	LPDDR4_1_CH1_DQS_C_B[1]	IO_L6N_GC_XCC_N2P1_M1P67_704	1.1	704
BH27	LPDDR4_1_CH1_DQS_T_A[0]	IO_L9P_GC_XCC_N3P0_M1P126_705	1.1	705
AY24	LPDDR4_1_CH1_DQS_T_A[1]	IO_L21P_XCC_N7P0_M1P96_704	1.1	704
AT29	LPDDR4_1_CH1_DQS_T_B[0]	IO_L18P_XCC_N6P0_M1P144_705	1.1	705
BG26	LPDDR4_1_CH1_DQS_T_B[1]	IO_L6P_GC_XCC_N2P0_M1P66_704	1.1	704

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage	Bank
BF19	LPDDR4_1_CH1_RESET_N[0]	IO_L25N_N8P3_M1P51_703	1.1	703
AV34	LPDDR4_2_CH0_CA_A[0]	IO_L22N_N7P3_M2P45_706	1.1	706
AU35	LPDDR4_2_CH0_CA_A[1]	IO_L22P_N7P2_M2P44_706	1.1	706
AV31	LPDDR4_2_CH0_CA_A[2]	IO_L21P_XCC_N7P0_M2P42_706	1.1	706
AW32	LPDDR4_2_CH0_CA_A[3]	IO_L23N_N7P5_M2P47_706	1.1	706
AT31	LPDDR4_2_CH0_CA_A[4]	IO_L19P_N6P2_M2P38_706	1.1	706
AU32	LPDDR4_2_CH0_CA_A[5]	IO_L19N_N6P3_M2P39_706	1.1	706
BA33	LPDDR4_2_CH0_CA_B[0]	IO_L16P_N5P2_M2P32_706	1.1	706
AY35	LPDDR4_2_CH0_CA_B[1]	IO_L14N_N4P5_M2P29_706	1.1	706
BC34	LPDDR4_2_CH0_CA_B[2]	IO_L17N_N5P5_M2P35_706	1.1	706
BB34	LPDDR4_2_CH0_CA_B[3]	IO_L17P_N5P4_M2P34_706	1.1	706
BA31	LPDDR4_2_CH0_CA_B[4]	IO_L13N_N4P3_M2P27_706	1.1	706
AY32	LPDDR4_2_CH0_CA_B[5]	IO_L13P_N4P2_M2P26_706	1.1	706
AT35	LPDDR4_2_CH0_CK_C_A[0]	IO_L18N_XCC_N6P1_M2P37_706	1.1	706
AY33	LPDDR4_2_CH0_CK_C_B[0]	IO_L12N_GC_XCC_N4P1_M2P25_706	1.1	706
AT34	LPDDR4_2_CH0_CK_T_A[0]	IO_L18P_XCC_N6P0_M2P36_706	1.1	706
AW34	LPDDR4_2_CH0_CK_T_B[0]	IO_L12P_GC_XCC_N4P0_M2P24_706	1.1	706
AT32	LPDDR4_2_CH0_CKE_A[0]	IO_L20P_N6P4_M2P40_706	1.1	706
AU33	LPDDR4_2_CH0_CKE_A[1]	IO_L20N_N6P5_M2P41_706	1.1	706
AW35	LPDDR4_2_CH0_CKE_B[0]	IO_L14P_N4P4_M2P28_706	1.1	706
BA34	LPDDR4_2_CH0_CKE_B[1]	IO_L16N_N5P3_M2P33_706	1.1	706
AV33	LPDDR4_2_CH0_CS_A[0]	IO_L23P_N7P4_M2P46_706	1.1	706
AW31	LPDDR4_2_CH0_CS_A[1]	IO_L21N_XCC_N7P1_M2P43_706	1.1	706
BM35	LPDDR4_2_CH0_CS_B[0]	IO_L0N_XCC_N0P1_M2P1_706	1.1	706
BG33	LPDDR4_2_CH0_CS_B[1]	IO_L9N_GC_XCC_N3P1_M2P19_706	1.1	706
BD38	LPDDR4_2_CH0_DMI_A[0]	IO_L15P_XCC_N5P0_M2P84_707	1.1	707
BG32	LPDDR4_2_CH0_DMI_A[1]	IO_L9P_GC_XCC_N3P0_M2P18_706	1.1	706
BC44	LPDDR4_2_CH0_DMI_B[0]	IO_L3P_XCC_N1P0_M2P60_707	1.1	707
BL34	LPDDR4_2_CH0_DMI_B[1]	IO_L0P_XCC_N0P0_M2P0_706	1.1	706
BA37	LPDDR4_2_CH0_DQ_A[0]	IO_L14N_N4P5_M2P83_707	1.1	707
BB39	LPDDR4_2_CH0_DQ_A[1]	IO_L16N_N5P3_M2P87_707	1.1	707
BF32	LPDDR4_2_CH0_DQ_A[10]	IO_L7N_N2P3_M2P15_706	1.1	706
BF31	LPDDR4_2_CH0_DQ_A[11]	IO_L7P_N2P2_M2P14_706	1.1	706
BJ32	LPDDR4_2_CH0_DQ_A[12]	IO_L11N_N3P5_M2P23_706	1.1	706
BH32	LPDDR4_2_CH0_DQ_A[13]	IO_L11P_N3P4_M2P22_706	1.1	706
BJ34	LPDDR4_2_CH0_DQ_A[14]	IO_L10N_N3P3_M2P21_706	1.1	706

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage	Bank
BH34	LPDDR4_2_CH0_DQ_A[15]	IO_L10P_N3P2_M2P20_706	1.1	706
BB38	LPDDR4_2_CH0_DQ_A[2]	IO_L16P_N5P2_M2P86_707	1.1	707
BE38	LPDDR4_2_CH0_DQ_A[3]	IO_L17N_N5P5_M2P89_707	1.1	707
BE37	LPDDR4_2_CH0_DQ_A[4]	IO_L17P_N5P4_M2P88_707	1.1	707
BA36	LPDDR4_2_CH0_DQ_A[5]	IO_L13N_N4P3_M2P81_707	1.1	707
BB35	LPDDR4_2_CH0_DQ_A[6]	IO_L13P_N4P2_M2P80_707	1.1	707
AY36	LPDDR4_2_CH0_DQ_A[7]	IO_L14P_N4P4_M2P82_707	1.1	707
BG35	LPDDR4_2_CH0_DQ_A[8]	IO_L8N_N2P5_M2P17_706	1.1	706
BF35	LPDDR4_2_CH0_DQ_A[9]	IO_L8P_N2P4_M2P16_706	1.1	706
BE44	LPDDR4_2_CH0_DQ_B[0]	IO_L5P_N1P4_M2P64_707	1.1	707
BD44	LPDDR4_2_CH0_DQ_B[1]	IO_L4N_N1P3_M2P63_707	1.1	707
BM34	LPDDR4_2_CH0_DQ_B[10]	IO_L4P_N1P2_M2P8_706	1.1	706
BN35	LPDDR4_2_CH0_DQ_B[11]	IO_L4N_N1P3_M2P9_706	1.1	706
BM32	LPDDR4_2_CH0_DQ_B[12]	IO_L5P_N1P4_M2P10_706	1.1	706
BN32	LPDDR4_2_CH0_DQ_B[13]	IO_L5N_N1P5_M2P11_706	1.1	706
BL33	LPDDR4_2_CH0_DQ_B[14]	IO_L1N_N0P3_M2P3_706	1.1	706
BJ33	LPDDR4_2_CH0_DQ_B[15]	IO_L2P_N0P4_M2P4_706	1.1	706
BE45	LPDDR4_2_CH0_DQ_B[2]	IO_L5N_N1P5_M2P65_707	1.1	707
BB42	LPDDR4_2_CH0_DQ_B[3]	IO_L2N_N0P5_M2P59_707	1.1	707
BC42	LPDDR4_2_CH0_DQ_B[4]	IO_L2P_N0P4_M2P58_707	1.1	707
BD42	LPDDR4_2_CH0_DQ_B[5]	IO_L1N_N0P3_M2P57_707	1.1	707
BE42	LPDDR4_2_CH0_DQ_B[6]	IO_L1P_N0P2_M2P56_707	1.1	707
BD43	LPDDR4_2_CH0_DQ_B[7]	IO_L4P_N1P2_M2P62_707	1.1	707
BK33	LPDDR4_2_CH0_DQ_B[8]	IO_L2N_N0P5_M2P5_706	1.1	706
BK32	LPDDR4_2_CH0_DQ_B[9]	IO_L1P_N0P2_M2P2_706	1.1	706
BC37	LPDDR4_2_CH0_DQS_C_A[0]	IO_L12N_GC_XCC_N4P1_M2P79_707	1.1	707
BG34	LPDDR4_2_CH0_DQS_C_A[1]	IO_L6N_GC_XCC_N2P1_M2P13_706	1.1	706
BB44	LPDDR4_2_CH0_DQS_C_B[0]	IO_L0N_XCC_N0P1_M2P55_707	1.1	707
BN34	LPDDR4_2_CH0_DQS_C_B[1]	IO_L3N_XCC_N1P1_M2P7_706	1.1	706
BB36	LPDDR4_2_CH0_DQS_T_A[0]	IO_L12P_GC_XCC_N4P0_M2P78_707	1.1	707
BF34	LPDDR4_2_CH0_DQS_T_A[1]	IO_L6P_GC_XCC_N2P0_M2P12_706	1.1	706
BB43	LPDDR4_2_CH0_DQS_T_B[0]	IO_L0P_XCC_N0P0_M2P54_707	1.1	707
BM33	LPDDR4_2_CH0_DQS_T_B[1]	IO_L3P_XCC_N1P0_M2P6_706	1.1	706
BD35	LPDDR4_2_CH0_RESET_N[0]	IO_L25P_N8P2_M2P50_706	1.1	706
AW45	LPDDR4_2_CH1_CA_A[0]	IO_L4N_N1P3_M2P117_708	1.1	708
AV44	LPDDR4_2_CH1_CA_A[1]	IO_L4P_N1P2_M2P116_708	1.1	708

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage	Bank
AW44	LPDDR4_2_CH1_CA_A[2]	IO_L5N_N1P5_M2P119_708	1.1	708
AV43	LPDDR4_2_CH1_CA_A[3]	IO_L5P_N1P4_M2P118_708	1.1	708
AT40	LPDDR4_2_CH1_CA_A[4]	IO_L1P_N0P2_M2P110_708	1.1	708
AU39	LPDDR4_2_CH1_CA_A[5]	IO_L1N_N0P3_M2P111_708	1.1	708
AH42	LPDDR4_2_CH1_CA_B[0]	IO_L14P_N4P4_M2P136_708	1.1	708
AJ42	LPDDR4_2_CH1_CA_B[1]	IO_L14N_N4P5_M2P137_708	1.1	708
AL41	LPDDR4_2_CH1_CA_B[2]	IO_L17N_N5P5_M2P143_708	1.1	708
AJ40	LPDDR4_2_CH1_CA_B[3]	IO_L13N_N4P3_M2P135_708	1.1	708
AH41	LPDDR4_2_CH1_CA_B[4]	IO_L13P_N4P2_M2P134_708	1.1	708
AK41	LPDDR4_2_CH1_CA_B[5]	IO_L17P_N5P4_M2P142_708	1.1	708
AU42	LPDDR4_2_CH1_CK_C_A[0]	IO_L0N_XCC_N0P1_M2P109_708	1.1	708
AJ43	LPDDR4_2_CH1_CK_C_B[0]	IO_L12N_GC_XCC_N4P1_M2P133_708	1.1	708
AT43	LPDDR4_2_CH1_CK_T_A[0]	IO_L0P_XCC_N0P0_M2P108_708	1.1	708
AH44	LPDDR4_2_CH1_CK_T_B[0]	IO_L12P_GC_XCC_N4P0_M2P132_708	1.1	708
AU44	LPDDR4_2_CH1_CKE_A[0]	IO_L2P_N0P4_M2P112_708	1.1	708
AW43	LPDDR4_2_CH1_CKE_A[1]	IO_L3N_XCC_N1P1_M2P115_708	1.1	708
AL39	LPDDR4_2_CH1_CKE_B[0]	IO_L15N_XCC_N5P1_M2P139_708	1.1	708
AK40	LPDDR4_2_CH1_CKE_B[1]	IO_L15P_XCC_N5P0_M2P138_708	1.1	708
AV42	LPDDR4_2_CH1_CS_A[0]	IO_L3P_XCC_N1P0_M2P114_708	1.1	708
AU45	LPDDR4_2_CH1_CS_A[1]	IO_L2N_N0P5_M2P113_708	1.1	708
AN41	LPDDR4_2_CH1_CS_B[0]	IO_L6N_GC_XCC_N2P1_M2P121_708	1.1	708
AG40	LPDDR4_2_CH1_CS_B[1]	IO_L21N_XCC_N7P1_M2P151_708	1.1	708
AM42	LPDDR4_2_CH1_DMI_A[0]	IO_L6P_GC_XCC_N2P0_M2P120_708	1.1	708
AU38	LPDDR4_2_CH1_DMI_A[1]	IO_L18P_XCC_N6P0_M2P90_707	1.1	707
AF39	LPDDR4_2_CH1_DMI_B[0]	IO_L21P_XCC_N7P0_M2P150_708	1.1	708
BA42	LPDDR4_2_CH1_DMI_B[1]	IO_L9P_GC_XCC_N3P0_M2P72_707	1.1	707
AR40	LPDDR4_2_CH1_DQ_A[0]	IO_L11N_N3P5_M2P131_708	1.1	708
AR39	LPDDR4_2_CH1_DQ_A[1]	IO_L11P_N3P4_M2P130_708	1.1	708
AT37	LPDDR4_2_CH1_DQ_A[10]	IO_L20P_N6P4_M2P94_707	1.1	707
AT38	LPDDR4_2_CH1_DQ_A[11]	IO_L20N_N6P5_M2P95_707	1.1	707
AV36	LPDDR4_2_CH1_DQ_A[12]	IO_L23P_N7P4_M2P100_707	1.1	707
AU36	LPDDR4_2_CH1_DQ_A[13]	IO_L19P_N6P2_M2P92_707	1.1	707
AW37	LPDDR4_2_CH1_DQ_A[14]	IO_L23N_N7P5_M2P101_707	1.1	707
AV37	LPDDR4_2_CH1_DQ_A[15]	IO_L19N_N6P3_M2P93_707	1.1	707
AM40	LPDDR4_2_CH1_DQ_A[2]	IO_L7N_N2P3_M2P123_708	1.1	708
AM39	LPDDR4_2_CH1_DQ_A[3]	IO_L7P_N2P2_M2P122_708	1.1	708

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage	Bank
AP42	LPDDR4_2_CH1_DQ_A[4]	IO_L8N_N2P5_M2P125_708	1.1	708
AP41	LPDDR4_2_CH1_DQ_A[5]	IO_L8P_N2P4_M2P124_708	1.1	708
AT41	LPDDR4_2_CH1_DQ_A[6]	IO_L10P_N3P2_M2P128_708	1.1	708
AU41	LPDDR4_2_CH1_DQ_A[7]	IO_L10N_N3P3_M2P129_708	1.1	708
AY39	LPDDR4_2_CH1_DQ_A[8]	IO_L22N_N7P3_M2P99_707	1.1	707
AW38	LPDDR4_2_CH1_DQ_A[9]	IO_L22P_N7P2_M2P98_707	1.1	707
AD40	LPDDR4_2_CH1_DQ_B[0]	IO_L19P_N6P2_M2P146_708	1.1	708
AF40	LPDDR4_2_CH1_DQ_B[1]	IO_L22P_N7P2_M2P152_708	1.1	708
AY41	LPDDR4_2_CH1_DQ_B[10]	IO_L7N_N2P3_M2P69_707	1.1	707
AY45	LPDDR4_2_CH1_DQ_B[11]	IO_L11N_N3P5_M2P77_707	1.1	707
BA45	LPDDR4_2_CH1_DQ_B[12]	IO_L11P_N3P4_M2P76_707	1.1	707
BA44	LPDDR4_2_CH1_DQ_B[13]	IO_L10N_N3P3_M2P75_707	1.1	707
BA43	LPDDR4_2_CH1_DQ_B[14]	IO_L10P_N3P2_M2P74_707	1.1	707
AV40	LPDDR4_2_CH1_DQ_B[15]	IO_L8P_N2P4_M2P70_707	1.1	707
AE39	LPDDR4_2_CH1_DQ_B[2]	IO_L19N_N6P3_M2P147_708	1.1	708
AH39	LPDDR4_2_CH1_DQ_B[3]	IO_L23P_N7P4_M2P154_708	1.1	708
AJ39	LPDDR4_2_CH1_DQ_B[4]	IO_L23N_N7P5_M2P155_708	1.1	708
AG41	LPDDR4_2_CH1_DQ_B[5]	IO_L22N_N7P3_M2P153_708	1.1	708
AF42	LPDDR4_2_CH1_DQ_B[6]	IO_L20N_N6P5_M2P149_708	1.1	708
AE41	LPDDR4_2_CH1_DQ_B[7]	IO_L20P_N6P4_M2P148_708	1.1	708
AW40	LPDDR4_2_CH1_DQ_B[8]	IO_L7P_N2P2_M2P68_707	1.1	707
AW41	LPDDR4_2_CH1_DQ_B[9]	IO_L8N_N2P5_M2P71_707	1.1	707
AP39	LPDDR4_2_CH1_DQS_C_A[0]	IO_L9N_GC_XCC_N3P1_M2P127_708	1.1	708
BA39	LPDDR4_2_CH1_DQS_C_A[1]	IO_L21N_XCC_N7P1_M2P97_707	1.1	707
AE42	LPDDR4_2_CH1_DQS_C_B[0]	IO_L18N_XCC_N6P1_M2P145_708	1.1	708
BA40	LPDDR4_2_CH1_DQS_C_B[1]	IO_L6N_GC_XCC_N2P1_M2P67_707	1.1	707
AN40	LPDDR4_2_CH1_DQS_T_A[0]	IO_L9P_GC_XCC_N3P0_M2P126_708	1.1	708
AY38	LPDDR4_2_CH1_DQS_T_A[1]	IO_L21P_XCC_N7P0_M2P96_707	1.1	707
AD41	LPDDR4_2_CH1_DQS_T_B[0]	IO_L18P_XCC_N6P0_M2P144_708	1.1	708
BB40	LPDDR4_2_CH1_DQS_T_B[1]	IO_L6P_GC_XCC_N2P0_M2P66_707	1.1	707
BE34	LPDDR4_2_CH1_RESET_N[0]	IO_L25N_N8P3_M2P51_706	1.1	706
B31	LPDDR4_3_CH0_CA_A[0]	IO_L1N_N0P3_M3P111_711	1.1	711
C31	LPDDR4_3_CH0_CA_A[1]	IO_L1P_N0P2_M3P110_711	1.1	711
C32	LPDDR4_3_CH0_CA_A[2]	IO_L0P_XCC_N0P0_M3P108_711	1.1	711
C29	LPDDR4_3_CH0_CA_A[3]	IO_L2N_N0P5_M3P113_711	1.1	711
B29	LPDDR4_3_CH0_CA_A[4]	IO_L4P_N1P2_M3P116_711	1.1	711

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage	Bank
A29	LPDDR4_3_CH0_CA_A[5]	IO_L4N_N1P3_M3P117_711	1.1	711
F30	LPDDR4_3_CH0_CA_B[0]	IO_L7P_N2P2_M3P122_711	1.1	711
D33	LPDDR4_3_CH0_CA_B[1]	IO_L11N_N3P5_M3P131_711	1.1	711
D32	LPDDR4_3_CH0_CA_B[2]	IO_L8N_N2P5_M3P125_711	1.1	711
E31	LPDDR4_3_CH0_CA_B[3]	IO_L8P_N2P4_M3P124_711	1.1	711
D34	LPDDR4_3_CH0_CA_B[4]	IO_L10N_N3P3_M3P129_711	1.1	711
E33	LPDDR4_3_CH0_CA_B[5]	IO_L10P_N3P2_M3P128_711	1.1	711
A33	LPDDR4_3_CH0_CK_C_A[0]	IO_L3N_XCC_N1P1_M3P115_711	1.1	711
C30	LPDDR4_3_CH0_CK_C_B[0]	IO_L9N_GC_XCC_N3P1_M3P127_711	1.1	711
B33	LPDDR4_3_CH0_CK_T_A[0]	IO_L3P_XCC_N1P0_M3P114_711	1.1	711
D30	LPDDR4_3_CH0_CK_T_B[0]	IO_L9P_GC_XCC_N3P0_M3P126_711	1.1	711
A31	LPDDR4_3_CH0_CKE_A[0]	IO_L5P_N1P4_M3P118_711	1.1	711
A30	LPDDR4_3_CH0_CKE_A[1]	IO_L5N_N1P5_M3P119_711	1.1	711
E32	LPDDR4_3_CH0_CKE_B[0]	IO_L11P_N3P4_M3P130_711	1.1	711
E30	LPDDR4_3_CH0_CKE_B[1]	IO_L7N_N2P3_M3P123_711	1.1	711
D29	LPDDR4_3_CH0_CS_A[0]	IO_L2P_N0P4_M3P112_711	1.1	711
B32	LPDDR4_3_CH0_CS_A[1]	IO_L0N_XCC_N0P1_M3P109_711	1.1	711
R30	LPDDR4_3_CH0_CS_B[0]	IO_L21N_XCC_N7P1_M3P151_711	1.1	711
M31	LPDDR4_3_CH0_CS_B[1]	IO_L12N_GC_XCC_N4P1_M3P133_711	1.1	711
G26	LPDDR4_3_CH0_DMI_A[0]	IO_L6P_GC_XCC_N2P0_M3P66_710	1.1	710
N31	LPDDR4_3_CH0_DMI_A[1]	IO_L12P_GC_XCC_N4P0_M3P132_711	1.1	711
V25	LPDDR4_3_CH0_DMI_B[0]	IO_L18P_XCC_N6P0_M3P90_710	1.1	710
T30	LPDDR4_3_CH0_DMI_B[1]	IO_L21P_XCC_N7P0_M3P150_711	1.1	711
A25	LPDDR4_3_CH0_DQ_A[0]	IO_L11N_N3P5_M3P77_710	1.1	710
E25	LPDDR4_3_CH0_DQ_A[1]	IO_L8N_N2P5_M3P71_710	1.1	710
L29	LPDDR4_3_CH0_DQ_A[10]	IO_L13N_N4P3_M3P135_711	1.1	711
M29	LPDDR4_3_CH0_DQ_A[11]	IO_L13P_N4P2_M3P134_711	1.1	711
L30	LPDDR4_3_CH0_DQ_A[12]	IO_L14P_N4P4_M3P136_711	1.1	711
K30	LPDDR4_3_CH0_DQ_A[13]	IO_L14N_N4P5_M3P137_711	1.1	711
J30	LPDDR4_3_CH0_DQ_A[14]	IO_L17P_N5P4_M3P142_711	1.1	711
H30	LPDDR4_3_CH0_DQ_A[15]	IO_L17N_N5P5_M3P143_711	1.1	711
A26	LPDDR4_3_CH0_DQ_A[2]	IO_L10N_N3P3_M3P75_710	1.1	710
B26	LPDDR4_3_CH0_DQ_A[3]	IO_L11P_N3P4_M3P76_710	1.1	710
E27	LPDDR4_3_CH0_DQ_A[4]	IO_L7P_N2P2_M3P68_710	1.1	710
E26	LPDDR4_3_CH0_DQ_A[5]	IO_L7N_N2P3_M3P69_710	1.1	710
F25	LPDDR4_3_CH0_DQ_A[6]	IO_L8P_N2P4_M3P70_710	1.1	710

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage	Bank
B27	LPDDR4_3_CH0_DQ_A[7]	IO_L10P_N3P2_M3P74_710	1.1	710
H29	LPDDR4_3_CH0_DQ_A[8]	IO_L16N_N5P3_M3P141_711	1.1	711
J29	LPDDR4_3_CH0_DQ_A[9]	IO_L16P_N5P2_M3P140_711	1.1	711
M27	LPDDR4_3_CH0_DQ_B[0]	IO_L22P_N7P2_M3P98_710	1.1	710
M26	LPDDR4_3_CH0_DQ_B[1]	IO_L23P_N7P4_M3P100_710	1.1	710
P29	LPDDR4_3_CH0_DQ_B[10]	IO_L23P_N7P4_M3P154_711	1.1	711
P30	LPDDR4_3_CH0_DQ_B[11]	IO_L22P_N7P2_M3P152_711	1.1	711
T28	LPDDR4_3_CH0_DQ_B[12]	IO_L20N_N6P5_M3P149_711	1.1	711
T29	LPDDR4_3_CH0_DQ_B[13]	IO_L19N_N6P3_M3P147_711	1.1	711
U28	LPDDR4_3_CH0_DQ_B[14]	IO_L20P_N6P4_M3P148_711	1.1	711
U29	LPDDR4_3_CH0_DQ_B[15]	IO_L19P_N6P2_M3P146_711	1.1	711
L26	LPDDR4_3_CH0_DQ_B[2]	IO_L22N_N7P3_M3P99_710	1.1	710
L25	LPDDR4_3_CH0_DQ_B[3]	IO_L23N_N7P5_M3P101_710	1.1	710
P25	LPDDR4_3_CH0_DQ_B[4]	IO_L20N_N6P5_M3P95_710	1.1	710
U24	LPDDR4_3_CH0_DQ_B[5]	IO_L19P_N6P2_M3P92_710	1.1	710
T25	LPDDR4_3_CH0_DQ_B[6]	IO_L19N_N6P3_M3P93_710	1.1	710
R25	LPDDR4_3_CH0_DQ_B[7]	IO_L20P_N6P4_M3P94_710	1.1	710
N30	LPDDR4_3_CH0_DQ_B[8]	IO_L22N_N7P3_M3P153_711	1.1	711
N29	LPDDR4_3_CH0_DQ_B[9]	IO_L23N_N7P5_M3P155_711	1.1	711
C25	LPDDR4_3_CH0_DQS_C_A[0]	IO_L9N_GC_XCC_N3P1_M3P73_710	1.1	710
K31	LPDDR4_3_CH0_DQS_C_A[1]	IO_L15N_XCC_N5P1_M3P139_711	1.1	711
N25	LPDDR4_3_CH0_DQS_C_B[0]	IO_L21N_XCC_N7P1_M3P97_710	1.1	710
V29	LPDDR4_3_CH0_DQS_C_B[1]	IO_L18N_XCC_N6P1_M3P145_711	1.1	711
D25	LPDDR4_3_CH0_DQS_T_A[0]	IO_L9P_GC_XCC_N3P0_M3P72_710	1.1	710
L31	LPDDR4_3_CH0_DQS_T_A[1]	IO_L15P_XCC_N5P0_M3P138_711	1.1	711
N26	LPDDR4_3_CH0_DQS_T_B[0]	IO_L21P_XCC_N7P0_M3P96_710	1.1	710
V30	LPDDR4_3_CH0_DQS_T_B[1]	IO_L18P_XCC_N6P0_M3P144_711	1.1	711
H31	LPDDR4_3_CH0_RESET_N[0]	IO_L25P_N8P2_M3P158_711	1.1	711
U23	LPDDR4_3_CH1_CA_A[0]	IO_L19N_N6P3_M3P39_709	1.1	709
V22	LPDDR4_3_CH1_CA_A[1]	IO_L19P_N6P2_M3P38_709	1.1	709
T21	LPDDR4_3_CH1_CA_A[2]	IO_L20N_N6P5_M3P41_709	1.1	709
U22	LPDDR4_3_CH1_CA_A[3]	IO_L20P_N6P4_M3P40_709	1.1	709
T24	LPDDR4_3_CH1_CA_A[4]	IO_L22P_N7P2_M3P44_709	1.1	709
T23	LPDDR4_3_CH1_CA_A[5]	IO_L22N_N7P3_M3P45_709	1.1	709
E23	LPDDR4_3_CH1_CA_B[0]	IO_L11P_N3P4_M3P22_709	1.1	709
D23	LPDDR4_3_CH1_CA_B[1]	IO_L11N_N3P5_M3P23_709	1.1	709

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage	Bank
G22	LPDDR4_3_CH1_CA_B[2]	IO_L8N_N2P5_M3P17_709	1.1	709
E21	LPDDR4_3_CH1_CA_B[3]	IO_L10N_N3P3_M3P21_709	1.1	709
E22	LPDDR4_3_CH1_CA_B[4]	IO_L10P_N3P2_M3P20_709	1.1	709
G23	LPDDR4_3_CH1_CA_B[5]	IO_L8P_N2P4_M3P16_709	1.1	709
T20	LPDDR4_3_CH1_CK_C_A[0]	IO_L21N_XCC_N7P1_M3P43_709	1.1	709
F23	LPDDR4_3_CH1_CK_C_B[0]	IO_L9N_GC_XCC_N3P1_M3P19_709	1.1	709
U21	LPDDR4_3_CH1_CK_T_A[0]	IO_L21P_XCC_N7P0_M3P42_709	1.1	709
F24	LPDDR4_3_CH1_CK_T_B[0]	IO_L9P_GC_XCC_N3P0_M3P18_709	1.1	709
R20	LPDDR4_3_CH1_CKE_A[0]	IO_L23P_N7P4_M3P46_709	1.1	709
V20	LPDDR4_3_CH1_CKE_A[1]	IO_L18N_XCC_N6P1_M3P37_709	1.1	709
J23	LPDDR4_3_CH1_CKE_B[0]	IO_L6N_GC_XCC_N2P1_M3P13_709	1.1	709
K23	LPDDR4_3_CH1_CKE_B[1]	IO_L6P_GC_XCC_N2P0_M3P12_709	1.1	709
V21	LPDDR4_3_CH1_CS_A[0]	IO_L18P_XCC_N6P0_M3P36_709	1.1	709
P20	LPDDR4_3_CH1_CS_A[1]	IO_L23N_N7P5_M3P47_709	1.1	709
M22	LPDDR4_3_CH1_CS_B[0]	IO_L15N_XCC_N5P1_M3P31_709	1.1	709
C21	LPDDR4_3_CH1_CS_B[1]	IO_L0N_XCC_N0P1_M3P1_709	1.1	709
N22	LPDDR4_3_CH1_DMI_A[0]	IO_L15P_XCC_N5P0_M3P30_709	1.1	709
D27	LPDDR4_3_CH1_DMI_A[1]	IO_L12P_GC_XCC_N4P0_M3P78_710	1.1	710
D22	LPDDR4_3_CH1_DMI_B[0]	IO_L0P_XCC_N0P0_M3P0_709	1.1	709
V27	LPDDR4_3_CH1_DMI_B[1]	IO_L3P_XCC_N1P0_M3P60_710	1.1	710
R22	LPDDR4_3_CH1_DQ_A[0]	IO_L13P_N4P2_M3P26_709	1.1	709
N21	LPDDR4_3_CH1_DQ_A[1]	IO_L17P_N5P4_M3P34_709	1.1	709
H27	LPDDR4_3_CH1_DQ_A[10]	IO_L13P_N4P2_M3P80_710	1.1	710
E28	LPDDR4_3_CH1_DQ_A[11]	IO_L14N_N4P5_M3P83_710	1.1	710
A28	LPDDR4_3_CH1_DQ_A[12]	IO_L17N_N5P5_M3P89_710	1.1	710
C27	LPDDR4_3_CH1_DQ_A[13]	IO_L16N_N5P3_M3P87_710	1.1	710
B28	LPDDR4_3_CH1_DQ_A[14]	IO_L17P_N5P4_M3P88_710	1.1	710
D28	LPDDR4_3_CH1_DQ_A[15]	IO_L16P_N5P2_M3P86_710	1.1	710
M21	LPDDR4_3_CH1_DQ_A[2]	IO_L17N_N5P5_M3P35_709	1.1	709
R23	LPDDR4_3_CH1_DQ_A[3]	IO_L14P_N4P4_M3P28_709	1.1	709
P24	LPDDR4_3_CH1_DQ_A[4]	IO_L14N_N4P5_M3P29_709	1.1	709
M23	LPDDR4_3_CH1_DQ_A[5]	IO_L16N_N5P3_M3P33_709	1.1	709
N24	LPDDR4_3_CH1_DQ_A[6]	IO_L16P_N5P2_M3P32_709	1.1	709
P23	LPDDR4_3_CH1_DQ_A[7]	IO_L13N_N4P3_M3P27_709	1.1	709
F28	LPDDR4_3_CH1_DQ_A[8]	IO_L14P_N4P4_M3P82_710	1.1	710
G28	LPDDR4_3_CH1_DQ_A[9]	IO_L13N_N4P3_M3P81_710	1.1	710

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage	Bank
A23	LPDDR4_3_CH1_DQ_B[0]	IO_L4N_N1P3_M3P9_709	1.1	709
D24	LPDDR4_3_CH1_DQ_B[1]	IO_L1P_N0P2_M3P2_709	1.1	709
N27	LPDDR4_3_CH1_DQ_B[10]	IO_L5P_N1P4_M3P64_710	1.1	710
M28	LPDDR4_3_CH1_DQ_B[11]	IO_L5N_N1P5_M3P65_710	1.1	710
V26	LPDDR4_3_CH1_DQ_B[12]	IO_L1P_N0P2_M3P56_710	1.1	710
U26	LPDDR4_3_CH1_DQ_B[13]	IO_L1N_N0P3_M3P57_710	1.1	710
T26	LPDDR4_3_CH1_DQ_B[14]	IO_L2P_N0P4_M3P58_710	1.1	710
R26	LPDDR4_3_CH1_DQ_B[15]	IO_L2N_N0P5_M3P59_710	1.1	710
B22	LPDDR4_3_CH1_DQ_B[2]	IO_L2N_N0P5_M3P5_709	1.1	709
C22	LPDDR4_3_CH1_DQ_B[3]	IO_L2P_N0P4_M3P4_709	1.1	709
A24	LPDDR4_3_CH1_DQ_B[4]	IO_L5N_N1P5_M3P11_709	1.1	709
C24	LPDDR4_3_CH1_DQ_B[5]	IO_L1N_N0P3_M3P3_709	1.1	709
B23	LPDDR4_3_CH1_DQ_B[6]	IO_L4P_N1P2_M3P8_709	1.1	709
B24	LPDDR4_3_CH1_DQ_B[7]	IO_L5P_N1P4_M3P10_709	1.1	709
P28	LPDDR4_3_CH1_DQ_B[8]	IO_L4N_N1P3_M3P63_710	1.1	710
R28	LPDDR4_3_CH1_DQ_B[9]	IO_L4P_N1P2_M3P62_710	1.1	710
P22	LPDDR4_3_CH1_DQS_C_A[0]	IO_L12N_GC_XCC_N4P1_M3P25_709	1.1	709
G27	LPDDR4_3_CH1_DQS_C_A[1]	IO_L15N_XCC_N5P1_M3P85_710	1.1	710
A21	LPDDR4_3_CH1_DQS_C_B[0]	IO_L3N_XCC_N1P1_M3P7_709	1.1	709
P27	LPDDR4_3_CH1_DQS_C_B[1]	IO_L0N_XCC_N0P1_M3P55_710	1.1	710
R21	LPDDR4_3_CH1_DQS_T_A[0]	IO_L12P_GC_XCC_N4P0_M3P24_709	1.1	709
H26	LPDDR4_3_CH1_DQS_T_A[1]	IO_L15P_XCC_N5P0_M3P84_710	1.1	710
B21	LPDDR4_3_CH1_DQS_T_B[0]	IO_L3P_XCC_N1P0_M3P6_709	1.1	709
R27	LPDDR4_3_CH1_DQS_T_B[1]	IO_L0P_XCC_N0P0_M3P54_710	1.1	710
G32	LPDDR4_3_CH1_RESET_N[0]	IO_L25N_N8P3_M3P159_711	1.1	711
AU12	MEM_CLK_0_PIN_N	IO_L24N_GC_XCC_N8P1_M0P49_700	1.1	700
AT11	MEM_CLK_0_PIN_P	IO_L24P_GC_XCC_N8P0_M0P48_700	1.1	700
BD20	MEM_CLK_1_PIN_N	IO_L24N_GC_XCC_N8P1_M1P49_703	1.1	703
BC20	MEM_CLK_1_PIN_P	IO_L24P_GC_XCC_N8P0_M1P48_703	1.1	703
BE33	MEM_CLK_2_PIN_N	IO_L24N_GC_XCC_N8P1_M2P49_706	1.1	706
BE32	MEM_CLK_2_PIN_P	IO_L24P_GC_XCC_N8P0_M2P48_706	1.1	706
F31	MEM_CLK_3_PIN_N	IO_L24N_GC_XCC_N8P1_M3P157_711	1.1	711
G31	MEM_CLK_3_PIN_P	IO_L24P_GC_XCC_N8P0_M3P156_711	1.1	711
AB46	MGT_PROGCLK_0_PIN_N	GTM_REFCLKN0_204	MGT REFCLK	204
AB45	MGT_PROGCLK_0_PIN_P	GTM_REFCLKP0_204	MGT REFCLK	204
AF46	MGT_PROGCLK_1_PIN_N	GTM_REFCLKN0_203	MGT REFCLK	203

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage	Bank
AF45	MGT_PROGCLK_1_PIN_P	GTM_REFCLKP0_203	MGT REFCLK	203
AW48	MGT_PROGCLK_2_PIN_N	GTYP_REFCLKN0_200	MGT REFCLK	200
AW47	MGT_PROGCLK_2_PIN_P	GTYP_REFCLKP0_200	MGT REFCLK	200
AK8	PCIE_LCL_REFCLK_PIN_N	GTYP_LPD_REFCLKN0_103	MGT REFCLK	103
AK9	PCIE_LCL_REFCLK_PIN_P	GTYP_LPD_REFCLKP0_103	MGT REFCLK	103
AU6	PCIE_REFCLK_0_PIN_N	GTYP_LPD_REFCLKN0_102	MGT REFCLK	102
AU7	PCIE_REFCLK_0_PIN_P	GTYP_LPD_REFCLKP0_102	MGT REFCLK	102
AF8	PCIE_REFCLK_1_PIN_N	GTYP_LPD_REFCLKN0_104	MGT REFCLK	104
AF9	PCIE_REFCLK_1_PIN_P	GTYP_LPD_REFCLKP0_104	MGT REFCLK	104
W17	PCIE_RST_1V8_L	PMC_MIO38_501	1.8	501
W18	PCIE_RST_1V8_L	PMC_MIO39_501	1.8	501
BG1	PCIE_RX0_N	GTYP_LPD_RXN0_102	MGT	102
BG2	PCIE_RX0_P	GTYP_LPD_RXP0_102	MGT	102
BE1	PCIE_RX1_N	GTYP_LPD_RXN1_102	MGT	102
BE2	PCIE_RX1_P	GTYP_LPD_RXP1_102	MGT	102
AL1	PCIE_RX10_N	GTYP_LPD_RXN2_104	MGT	104
AL2	PCIE_RX10_P	GTYP_LPD_RXP2_104	MGT	104
AJ1	PCIE_RX11_N	GTYP_LPD_RXN3_104	MGT	104
AJ2	PCIE_RX11_P	GTYP_LPD_RXP3_104	MGT	104
AG1	PCIE_RX12_N	GTYP_LPD_RXN0_105	MGT	105
AG2	PCIE_RX12_P	GTYP_LPD_RXP0_105	MGT	105
AE1	PCIE_RX13_N	GTYP_LPD_RXN1_105	MGT	105
AE2	PCIE_RX13_P	GTYP_LPD_RXP1_105	MGT	105
AD3	PCIE_RX14_N	GTYP_LPD_RXN2_105	MGT	105
AD4	PCIE_RX14_P	GTYP_LPD_RXP2_105	MGT	105
AC1	PCIE_RX15_N	GTYP_LPD_RXN3_105	MGT	105
AC2	PCIE_RX15_P	GTYP_LPD_RXP3_105	MGT	105
BC1	PCIE_RX2_N	GTYP_LPD_RXN2_102	MGT	102
BC2	PCIE_RX2_P	GTYP_LPD_RXP2_102	MGT	102
BB3	PCIE_RX3_N	GTYP_LPD_RXN3_102	MGT	102
BB4	PCIE_RX3_P	GTYP_LPD_RXP3_102	MGT	102
BA1	PCIE_RX4_N	GTYP_LPD_RXN0_103	MGT	103
BA2	PCIE_RX4_P	GTYP_LPD_RXP0_103	MGT	103
AY3	PCIE_RX5_N	GTYP_LPD_RXN1_103	MGT	103
AY4	PCIE_RX5_P	GTYP_LPD_RXP1_103	MGT	103
AW1	PCIE_RX6_N	GTYP_LPD_RXN2_103	MGT	103

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage	Bank
AW2	PCIE_RX6_P	GTYP_LPD_RXP2_103	MGT	103
AU1	PCIE_RX7_N	GTYP_LPD_RXN3_103	MGT	103
AU2	PCIE_RX7_P	GTYP_LPD_RXP3_103	MGT	103
AR1	PCIE_RX8_N	GTYP_LPD_RXN0_104	MGT	104
AR2	PCIE_RX8_P	GTYP_LPD_RXP0_104	MGT	104
AN1	PCIE_RX9_N	GTYP_LPD_RXN1_104	MGT	104
AN2	PCIE_RX9_P	GTYP_LPD_RXP1_104	MGT	104
BG6	PCIE_TX0_PIN_N	GTYP_LPD_TXN0_102	MGT	102
BG7	PCIE_TX0_PIN_P	GTYP_LPD_TXP0_102	MGT	102
BF4	PCIE_TX1_PIN_N	GTYP_LPD_TXN1_102	MGT	102
BF5	PCIE_TX1_PIN_P	GTYP_LPD_TXP1_102	MGT	102
AP4	PCIE_TX10_PIN_N	GTYP_LPD_TXN2_104	MGT	104
AP5	PCIE_TX10_PIN_P	GTYP_LPD_TXP2_104	MGT	104
AN6	PCIE_TX11_PIN_N	GTYP_LPD_TXN3_104	MGT	104
AN7	PCIE_TX11_PIN_P	GTYP_LPD_TXP3_104	MGT	104
AM4	PCIE_TX12_PIN_N	GTYP_LPD_TXN0_105	MGT	105
AM5	PCIE_TX12_PIN_P	GTYP_LPD_TXP0_105	MGT	105
AL6	PCIE_TX13_PIN_N	GTYP_LPD_TXN1_105	MGT	105
AL7	PCIE_TX13_PIN_P	GTYP_LPD_TXP1_105	MGT	105
AK4	PCIE_TX14_PIN_N	GTYP_LPD_TXN2_105	MGT	105
AK5	PCIE_TX14_PIN_P	GTYP_LPD_TXP2_105	MGT	105
AJ6	PCIE_TX15_PIN_N	GTYP_LPD_TXN3_105	MGT	105
AJ7	PCIE_TX15_PIN_P	GTYP_LPD_TXP3_105	MGT	105
BE6	PCIE_TX2_PIN_N	GTYP_LPD_TXN2_102	MGT	102
BE7	PCIE_TX2_PIN_P	GTYP_LPD_TXP2_102	MGT	102
BD4	PCIE_TX3_PIN_N	GTYP_LPD_TXN3_102	MGT	102
BD5	PCIE_TX3_PIN_P	GTYP_LPD_TXP3_102	MGT	102
BC6	PCIE_TX4_PIN_N	GTYP_LPD_TXN0_103	MGT	103
BC7	PCIE_TX4_PIN_P	GTYP_LPD_TXP0_103	MGT	103
BA6	PCIE_TX5_PIN_N	GTYP_LPD_TXN1_103	MGT	103
BA7	PCIE_TX5_PIN_P	GTYP_LPD_TXP1_103	MGT	103
AW6	PCIE_TX6_PIN_N	GTYP_LPD_TXN2_103	MGT	103
AW7	PCIE_TX6_PIN_P	GTYP_LPD_TXP2_103	MGT	103
AV4	PCIE_TX7_PIN_N	GTYP_LPD_TXN3_103	MGT	103
AV5	PCIE_TX7_PIN_P	GTYP_LPD_TXP3_103	MGT	103
AT4	PCIE_TX8_PIN_N	GTYP_LPD_TXN0_104	MGT	104

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage	Bank
AT5	PCIE_TX8_PIN_P	GTYP_LPD_TXP0_104	MGT	104
AR6	PCIE_TX9_PIN_N	GTYP_LPD_TXN1_104	MGT	104
AR7	PCIE_TX9_PIN_P	GTYP_LPD_TXP1_104	MGT	104
L35	PERST_PL_L	IO_L8N_N2P5_712	1.5	712
V36	PMOD_IO1_1V5	IO_L20P_N6P4_712	1.5	712
U36	PMOD_IO2_1V5	IO_L20N_N6P5_712	1.5	712
V31	PMOD_IO3_1V5	IO_L21P_XCC_N7P0_712	1.5	712
U31	PMOD_IO4_1V5	IO_L21N_XCC_N7P1_712	1.5	712
V37	PMOD_IO5_1V5	IO_L22P_N7P2_712	1.5	712
U37	PMOD_IO6_1V5	IO_L22N_N7P3_712	1.5	712
U33	PMOD_IO7_1V5	IO_L23P_N7P4_712	1.5	712
T33	PMOD_IO8_1V5	IO_L23N_N7P5_712	1.5	712
L21	QSFP0_LPMODE_1V1	IO_L26P_N8P4_M3P52_709	1.1	709
K22	QSFP0_RESET_1V1_L	IO_L25N_N8P3_M3P51_709	1.1	709
BL44	QSFP0_RX0_N	GTYP_RXN0_201	MGT	201
BK44	QSFP0_RX0_P	GTYP_RXP0_201	MGT	201
BN45	QSFP0_RX1_N	GTYP_RXN1_201	MGT	201
BM45	QSFP0_RX1_P	GTYP_RXP1_201	MGT	201
BL46	QSFP0_RX2_N	GTYP_RXN2_201	MGT	201
BK46	QSFP0_RX2_P	GTYP_RXP2_201	MGT	201
BN47	QSFP0_RX3_N	GTYP_RXN3_201	MGT	201
BM47	QSFP0_RX3_P	GTYP_RXP3_201	MGT	201
BN37	QSFP0_RX4_N	GTYP_RXN0_200	MGT	200
BM37	QSFP0_RX4_P	GTYP_RXP0_200	MGT	200
BN39	QSFP0_RX5_N	GTYP_RXN1_200	MGT	200
BM39	QSFP0_RX5_P	GTYP_RXP1_200	MGT	200
BN41	QSFP0_RX6_N	GTYP_RXN2_200	MGT	200
BM41	QSFP0_RX6_P	GTYP_RXP2_200	MGT	200
BN43	QSFP0_RX7_N	GTYP_RXN3_200	MGT	200
BM43	QSFP0_RX7_P	GTYP_RXP3_200	MGT	200
R36	QSFP0_SCL	IO_L14N_N4P5_712	1.5	712
T36	QSFP0_SDA	IO_L14P_N4P4_712	1.5	712
BK40	QSFP0_TX0_N	GTYP_TXN0_201	MGT	201
BJ40	QSFP0_TX0_P	GTYP_TXP0_201	MGT	201
BH41	QSFP0_TX1_N	GTYP_TXN1_201	MGT	201
BG41	QSFP0_TX1_P	GTYP_TXP1_201	MGT	201

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage	Bank
BK42	QSFP0_TX2_N	GTYP_TXN2_201	MGT	201
BJ42	QSFP0_TX2_P	GTYP_TXP2_201	MGT	201
BH43	QSFP0_TX3_N	GTYP_TXN3_201	MGT	201
BG43	QSFP0_TX3_P	GTYP_TXP3_201	MGT	201
BK36	QSFP0_TX4_N	GTYP_TXN0_200	MGT	200
BJ36	QSFP0_TX4_P	GTYP_TXP0_200	MGT	200
BH37	QSFP0_TX5_N	GTYP_TXN1_200	MGT	200
BG37	QSFP0_TX5_P	GTYP_TXP1_200	MGT	200
BK38	QSFP0_TX6_N	GTYP_TXN2_200	MGT	200
BJ38	QSFP0_TX6_P	GTYP_TXP2_200	MGT	200
BH39	QSFP0_TX7_N	GTYP_TXN3_200	MGT	200
BG39	QSFP0_TX7_P	GTYP_TXP3_200	MGT	200
J25	QSFP1_LPMODE_1V1	IO_L26P_N8P4_M3P106_710	1.1	710
J27	QSFP1_RESET_1V1_L	IO_L25N_N8P3_M3P105_710	1.1	710
BN49	QSFP1_RX0_N	GTM_RXN0_202	MGT	202
BM49	QSFP1_RX0_P	GTM_RXP0_202	MGT	202
BK51	QSFP1_RX1_N	GTM_RXN1_202	MGT	202
BK50	QSFP1_RX1_P	GTM_RXP1_202	MGT	202
BJ53	QSFP1_RX2_N	GTM_RXN2_202	MGT	202
BJ52	QSFP1_RX2_P	GTM_RXP2_202	MGT	202
BH51	QSFP1_RX3_N	GTM_RXN3_202	MGT	202
BH50	QSFP1_RX3_P	GTM_RXP3_202	MGT	202
BG53	QSFP1_RX4_N	GTM_RXN0_203	MGT	203
BG52	QSFP1_RX4_P	GTM_RXP0_203	MGT	203
BE53	QSFP1_RX5_N	GTM_RXN1_203	MGT	203
BE52	QSFP1_RX5_P	GTM_RXP1_203	MGT	203
BC53	QSFP1_RX6_N	GTM_RXN2_203	MGT	203
BC52	QSFP1_RX6_P	GTM_RXP2_203	MGT	203
BA53	QSFP1_RX7_N	GTM_RXN3_203	MGT	203
BA52	QSFP1_RX7_P	GTM_RXP3_203	MGT	203
R33	QSFP1_SCL	IO_L15P_XCC_N5P0_712	1.5	712
P33	QSFP1_SDA	IO_L15N_XCC_N5P1_712	1.5	712
BH45	QSFP1_TX0_N	GTM_TXN0_202	MGT	202
BG45	QSFP1_TX0_P	GTM_TXP0_202	MGT	202
BH47	QSFP1_TX1_N	GTM_TXN1_202	MGT	202
BG47	QSFP1_TX1_P	GTM_TXP1_202	MGT	202

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage	Bank
BK48	QSFP1_TX2_N	GTM_TXN2_202	MGT	202
BJ48	QSFP1_TX2_P	GTM_TXP2_202	MGT	202
BF50	QSFP1_TX3_N	GTM_TXN3_202	MGT	202
BF49	QSFP1_TX3_P	GTM_TXP3_202	MGT	202
BE48	QSFP1_TX4_N	GTM_TXN0_203	MGT	203
BE47	QSFP1_TX4_P	GTM_TXP0_203	MGT	203
BD50	QSFP1_TX5_N	GTM_TXN1_203	MGT	203
BD49	QSFP1_TX5_P	GTM_TXP1_203	MGT	203
BC48	QSFP1_TX6_N	GTM_TXN2_203	MGT	203
BC47	QSFP1_TX6_P	GTM_TXP2_203	MGT	203
BB50	QSFP1_TX7_N	GTM_TXN3_203	MGT	203
BB49	QSFP1_TX7_P	GTM_TXP3_203	MGT	203
AN44	QSFP2_LPMODE_1V1	IO_L26P_N8P4_M2P160_708	1.1	708
AN43	QSFP2_RESET_1V1_L	IO_L25N_N8P3_M2P159_708	1.1	708
AL53	QSFP2_RX0_N	GTM_RXN0_205	MGT	205
AL52	QSFP2_RX0_P	GTM_RXP0_205	MGT	205
AJ53	QSFP2_RX1_N	GTM_RXN1_205	MGT	205
AJ52	QSFP2_RX1_P	GTM_RXP1_205	MGT	205
AG53	QSFP2_RX2_N	GTM_RXN2_205	MGT	205
AG52	QSFP2_RX2_P	GTM_RXP2_205	MGT	205
AE53	QSFP2_RX3_N	GTM_RXN3_205	MGT	205
AE52	QSFP2_RX3_P	GTM_RXP3_205	MGT	205
AW53	QSFP2_RX4_N	GTM_RXN0_204	MGT	204
AW52	QSFP2_RX4_P	GTM_RXP0_204	MGT	204
AU53	QSFP2_RX5_N	GTM_RXN1_204	MGT	204
AU52	QSFP2_RX5_P	GTM_RXP1_204	MGT	204
AR53	QSFP2_RX6_N	GTM_RXN2_204	MGT	204
AR52	QSFP2_RX6_P	GTM_RXP2_204	MGT	204
AN53	QSFP2_RX7_N	GTM_RXN3_204	MGT	204
AN52	QSFP2_RX7_P	GTM_RXP3_204	MGT	204
R37	QSFP2_SCL	IO_L16P_N5P2_712	1.5	712
P37	QSFP2_SDA	IO_L16N_N5P3_712	1.5	712
AP50	QSFP2_TX0_N	GTM_TXN0_205	MGT	205
AP49	QSFP2_TX0_P	GTM_TXP0_205	MGT	205
AM50	QSFP2_TX1_N	GTM_TXN1_205	MGT	205
AM49	QSFP2_TX1_P	GTM_TXP1_205	MGT	205

Table 12 : Complete Pinout Table **(continued on next page)**

Pin Number	Signal Name	Pin Name	IO Voltage	Bank
AK50	QSFP2_TX2_N	GTM_TXN2_205	MGT	205
AK49	QSFP2_TX2_P	GTM_TXP2_205	MGT	205
AH50	QSFP2_TX3_N	GTM_TXN3_205	MGT	205
AH49	QSFP2_TX3_P	GTM_TXP3_205	MGT	205
BA48	QSFP2_TX4_N	GTM_TXN0_204	MGT	204
BA47	QSFP2_TX4_P	GTM_TXP0_204	MGT	204
AY50	QSFP2_TX5_N	GTM_TXN1_204	MGT	204
AY49	QSFP2_TX5_P	GTM_TXP1_204	MGT	204
AV50	QSFP2_TX6_N	GTM_TXN2_204	MGT	204
AV49	QSFP2_TX6_P	GTM_TXP2_204	MGT	204
AT50	QSFP2_TX7_N	GTM_TXN3_204	MGT	204
AT49	QSFP2_TX7_P	GTM_TXP3_204	MGT	204
J13	QSPI0_CLK_PIN	PMC_MIO0_500	1.8	500
R13	QSPI0_CS_B	PMC_MIO5_500	1.8	500
P13	QSPI0_IO[0]	PMC_MIO4_500	1.8	500
K13	QSPI0_IO[1]	PMC_MIO1_500	1.8	500
L13	QSPI0_IO[2]	PMC_MIO2_500	1.8	500
M13	QSPI0_IO[3]	PMC_MIO3_500	1.8	500
N14	QSPI1_CLK_PIN	PMC_MIO12_500	1.8	500
U13	QSPI1_CS_B	PMC_MIO7_500	1.8	500
V14	QSPI1_IO[0]	PMC_MIO8_500	1.8	500
U14	QSPI1_IO[1]	PMC_MIO9_500	1.8	500
T14	QSPI1_IO[2]	PMC_MIO10_500	1.8	500
P14	QSPI1_IO[3]	PMC_MIO11_500	1.8	500
T16	SDIO_1V8_CLK_PIN	PMC_MIO26_501	1.8	501
M16	SDIO_1V8_CMD	PMC_MIO29_501	1.8	501
L16	SDIO_1V8_DAT0	PMC_MIO30_501	1.8	501
K16	SDIO_1V8_DAT1	PMC_MIO31_501	1.8	501
M17	SDIO_1V8_DAT2	PMC_MIO32_501	1.8	501
N17	SDIO_1V8_DAT3	PMC_MIO33_501	1.8	501
N16	SDIO_1V8_DETECT	PMC_MIO28_501	1.8	501
P17	SDIO_1V8_SEL	PMC_MIO34_501	1.8	501
T34	SI5344_IN0_N	IO_L13N_N4P3_712	1.5	712
U34	SI5344_IN0_P	IO_L13P_N4P2_712	1.5	712
V35	SI5344_INTR_1V5_N	IO_L18P_XCC_N6P0_712	1.5	712
V32	SI5344_LOL_1V5_N	IO_L19P_N6P2_712	1.5	712

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage	Bank
U32	SI5344_LOL_XAXB_1V5_N	IO_L19N_N6P3_712	1.5	712
Y46	SI5344_OUT0_PIN_N	GTM_REFCLKN0_205	MGT REFCLK	205
Y45	SI5344_OUT0_PIN_P	GTM_REFCLKP0_205	MGT REFCLK	205
AJ48	SI5344_OUT1_PIN_N	GTM_REFCLKN0_202	MGT REFCLK	202
AJ47	SI5344_OUT1_PIN_P	GTM_REFCLKP0_202	MGT REFCLK	202
AR48	SI5344_OUT2_PIN_N	GTYP_REFCLKN0_201	MGT REFCLK	201
AR47	SI5344_OUT2_PIN_P	GTYP_REFCLKP0_201	MGT REFCLK	201
V34	SI5344_RST_1V5_N	IO_L18N_XCC_N6P1_712	1.5	712
R31	SI5344_SCL_1V5	IO_L17N_N5P5_712	1.5	712
T31	SI5344_SDA_1V5	IO_L17P_N5P4_712	1.5	712
M36	SI5402_1V5_SCL	IO_L8P_N2P4_712	1.5	712
M32	SI5402_1V5_SDA	IO_L7N_N2P3_712	1.5	712
K33	SI5402_GPIO0_1V5_N	IO_L5P_N1P4_712	1.5	712
J33	SI5402_GPIO1_1V5_N	IO_L5N_N1P5_712	1.5	712
N32	SI5402_GPIO2_1V5_N	IO_L7P_N2P2_712	1.5	712
J37	SI5402_IN0_N	IO_L4N_N1P3_712	1.5	712
J38	SI5402_IN0_P	IO_L4P_N1P2_712	1.5	712
J34	SI5402_IN1_N	IO_L3N_XCC_N1P1_712	1.5	712
J35	SI5402_IN1_P	IO_L3P_XCC_N1P0_712	1.5	712
K38	SI5402_IN2_N	IO_L2N_N0P5_712	1.5	712
L38	SI5402_IN2_P	IO_L2P_N0P4_712	1.5	712
AU48	SI5402_OUT1_PIN_N	GTYP_REFCLKN1_200	MGT REFCLK	200
AU47	SI5402_OUT1_PIN_P	GTYP_REFCLKP1_200	MGT REFCLK	200
AN48	SI5402_OUT2_PIN_N	GTYP_REFCLKN1_201	MGT REFCLK	201
AN47	SI5402_OUT2_PIN_P	GTYP_REFCLKP1_201	MGT REFCLK	201
AG48	SI5402_OUT3_PIN_N	GTM_REFCLKN1_202	MGT REFCLK	202
AG47	SI5402_OUT3_PIN_P	GTM_REFCLKP1_202	MGT REFCLK	202
AD46	SI5402_OUT4_PIN_N	GTM_REFCLKN1_203	MGT REFCLK	203
AD45	SI5402_OUT4_PIN_P	GTM_REFCLKP1_203	MGT REFCLK	203
M37	SI5402_OUT5_PIN_N	IO_L6N_GC_XCC_N2P1_712	1.5	712
N36	SI5402_OUT5_PIN_P	IO_L6P_GC_XCC_N2P0_712	1.5	712
AA44	SI5402_OUT6_PIN_N	GTM_REFCLKN1_204	MGT REFCLK	204
AA43	SI5402_OUT6_PIN_P	GTM_REFCLKP1_204	MGT REFCLK	204
W44	SI5402_OUT7_PIN_N	GTM_REFCLKN1_205	MGT REFCLK	205
W43	SI5402_OUT7_PIN_P	GTM_REFCLKP1_205	MGT REFCLK	205
K37	SI5402_RST_1V5_N	IO_L1N_N0P3_712	1.5	712

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage	Bank
BC41	SPARE_WP_1V1	IO_L26N_N8P5_M2P107_707	1.1	707
L34	SRVC_MD_L_1V5	IO_L9N_GC_XCC_N3P1_712	1.5	712
M38	TRIG_IN_FPGA	IO_L10N_N3P3_712	1.5	712
L33	TRIG_OUT_EN_FPGA	IO_L11N_N3P5_712	1.5	712
N34	TRIG_OUT_FPGA	IO_L25N_N8P3_712	1.5	712
P32	TRIG_TE_EN_FPGA	IO_L24N_GC_XCC_N8P1_712	1.5	712
R18	UART0_RXD	PMC_MIO42_501	1.8	501
P18	UART0_TXD	PMC_MIO43_501	1.8	501
P19	UART1_RXD	PMC_MIO47_501	1.8	501
N19	UART1_TXD	PMC_MIO46_501	1.8	501
L15	USB_ULPI_CLK_PIN	PMC_MIO18_500	1.8	500
L14	USB_ULPI_DATA[0]_PIN	PMC_MIO14_500	1.8	500
J14	USB_ULPI_DATA[1]_PIN	PMC_MIO15_500	1.8	500
J15	USB_ULPI_DATA[2]_PIN	PMC_MIO16_500	1.8	500
K15	USB_ULPI_DATA[3]_PIN	PMC_MIO17_500	1.8	500
N15	USB_ULPI_DATA[4]_PIN	PMC_MIO19_500	1.8	500
P15	USB_ULPI_DATA[5]_PIN	PMC_MIO20_500	1.8	500
R15	USB_ULPI_DATA[6]_PIN	PMC_MIO21_500	1.8	500
T15	USB_ULPI_DATA[7]_PIN	PMC_MIO22_500	1.8	500
V15	USB_ULPI_DIR_PIN	PMC_MIO23_500	1.8	500
U16	USB_ULPI_NXT_PIN	PMC_MIO25_500	1.8	500
M14	USB_ULPI_RST	PMC_MIO13_500	1.8	500
V16	USB_ULPI_STP_PIN	PMC_MIO24_500	1.8	500
BD30	USER_LED_G0_1V1	IO_L24P_GC_XCC_N8P0_M1P156_705	1.1	705
BE30	USER_LED_G1_1V1	IO_L24N_GC_XCC_N8P1_M1P157_705	1.1	705
BG29	USER_LED_G2_1V1	IO_L26N_N8P5_M1P161_705	1.1	705
BF28	USER_LED_G3_1V1	IO_L25N_N8P3_M1P159_705	1.1	705
BF30	USER_LED_G4_1V1	IO_L26P_N8P4_M1P160_705	1.1	705
BE29	USER_LED_G5_1V1	IO_L25P_N8P2_M1P158_705	1.1	705

Table 12 : Complete Pinout Table

Revision History

Date	Revision	Changed By	Nature of Change
30 Jun 2023	1.0	K. Roth	Initial Release.
17 Jul 2023	1.1	K. Roth	Clarifyied that ToD input is also 1PPS in Introduction, corrected multiple naming mistakes in Clock Topology, Correct blank cells within MIO Map, section Time of Day (ToD) / One Pulse per Second (1PPS) updated to include more detail.
18 Jul 2023	1.2	K. Roth	Changed references to FABRIC_CLK to also include refclk_100m, correct drawing number
26 Oct 2023	1.3	K. Roth	Updated Thermal Performance, corrected SI5402 index numbers in Clock Topology, corrected switch index fir viitnide 1 in Switch Functions, corrected SW1 to SW2 in Boot Mode Selection, added time limit for battery change, added Fan Speed Control, added si5344 pre-configured information to section Si5344.
17 Nov 2023	1.4	K. Roth	Removed references to ITU-T and replaced with generic descriptions.
3 JAN 2024	1.5	K. Roth	Included IEC standards reference to section Battery.
24 May 2024	1.6	K. Roth	Modified section on mechanical requirements to become Installation Instructions.
12 Jun 2024	1.7	K. Roth	Added a box around the text "A battery is not included".
17 Jun 2024	1.8	K. Roth	Removed section on battery.
31 Dec 2024	2.0	K. Roth	Revised LPDDR4 pinout in Complete Pinout Table to match revision 3 and newer PCBs for older C1 PCBs please contact alpha data for details, LPDDR4 speed references changed from 3933 to 3733 to match Vivado tool options, and SI5402 customer support link added.
04 Feb 2025	2.1	K. Roth	LPDDR4 speed references changed from 3733 to 3900 to match Vivado tool options, several Si5344 references corrected to say SI5402.

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